ARM® Versatile™ Express Juno r2 Development Platform (V2M-Juno r2)

Technical Reference Manual

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ARM® Versatile™ Express Juno r2 Development Platform (V2M-Juno r2)

Technical Reference Manual

Release Information

Document History

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Product Status

The information in this document is Final, that is for a developed product.

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Conformance Notices

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling Versatile™ Express boards.

The motherboard generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the target board
- Reorient the receiving antenna
- Increase the distance between the equipment and the receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables be used.

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Appendix C Revisions

Preface

This preface introduces the *ARM® Versatile™ Express Juno r2 Development Platform (V2M-Juno r2) Technical Reference Manual*.

It contains the following:

- *About this book* on page 7.
- *Feedback* on page 10.

About this book

This book describes the ARM® Versatile™ Express Juno r2 Development Platform, that is, the V2M-Juno r2 motherboard. This development board contains the Juno r2 Development Platform SoC.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m* Identifies the major revision of the product, for example, r1.

p*n* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for experienced hardware and software developers to aid ARMv8-A software and tooling development in the Juno r2 ARM Development Platform SoC using the V2M-Juno r2 motherboard.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter introduces the Versatile™ Express V2M-Juno r2 motherboard.

Chapter 2 Hardware Description
This chapter describes the Versatile Express V2M-Juno r2 motherboard hardware.

Chapter 3 Configuration
This chapter describes the powerup and configuration process of the Versatile Express V2M-Juno r2 motherboard.

Chapter 4 Programmers Model
This chapter describes the programmers model of the Versatile Express V2M-Juno r2 motherboard.

Appendix A Signal Descriptions
This appendix describes the signals present at the interface connectors of the Versatile Express V2M-Juno r2 motherboard.

Appendix B Specifications
This appendix contains the electrical specifications of the Versatile Express V2M-Juno r2 motherboard.

Appendix C Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

`<and>`
Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

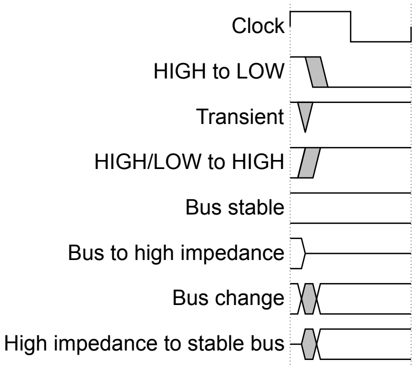

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n
At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

ARM publications

- *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* (ARM DDI 0515).
- *Juno ARM® Development Platform SoC Technical Overview (Revision r2p0)* (ARM DTO 0038)
- *AN415 Example Express 20MG design for a V2M-Juno Motherboard* (ARM DAI 0415).
- *ARM® LogicTile Express 3MG Technical Reference Manual* (ARM DUI 0449).
- *ARM® LogicTile Express 13MG Technical Reference Manual* (ARM DUI 0556).
- *ARM® LogicTile Express 20MG Technical Reference Manual* (ARM DDI 0498).
- *ARM® CoreLink™ TLX-400 Network Interconnect Thin Links Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0028).
- *ARM® PrimeCell Technical Reference Manual Real Time Clock (PL031)* (ARM DDI 0224).
- *ARM® PrimeCell PS2 Keyboard/Mouse Interface (PL050)* (ARM DDI 0143).
- *ARM® PrimeCell General Purpose Input/Output (PLO61)Technical Reference Manual* (ARM DUI 0142).
- *ARM® PrimeCell Multimedia Card Interface (PL180)Technical Reference Manual* (ARM DDI 0172).
- *ARM® Dual-Timer Module (SP804) Technical Reference Manual* (ARM DDI 0271).
- *ARM® Watchdog Module (SP805) Technical Reference Manual* (ARM DDI 0270).
- *CoreLink SMC-35x Static Memory Controller Series Technical Reference Manual* (ARM DDI 0380).
- *AMBA® 3 AHB-Lite Protocol Specification v1.0* (ARM IHI 0033).
- *AMBA® 3 APB Protocol Specification v1.0* (ARM IHI 000024).
- *ARM® DS-5 Setting up the ARM DSTREAM Hardware* (ARM DUI 0481).
- *ARM® DS-5 Using the Debug Hardware Configuration Utilities* (ARM DUI 0498).
- *CoreSight™ Components Technical Reference Manual* (ARM DDI 0314).
- *CoreSight™ Trace Memory Controller Technical Reference Manual* (ARM DDI 0461).

Other publications

- See the Linaro website *http://www.linaro.org/downloads/* for Linaro software.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *ARM® Versatile™ Express Juno r2 Development Platform (V2M-Juno r2) Technical Reference Manual*.
- The number ARM 100114_0200_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Note

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Chapter 1
Introduction

This chapter introduces the Versatile™ Express V2M-Juno r2 motherboard.

It contains the following sections:

1.1 Precautions

You can take certain precautions to ensure safety and to prevent damage to your V2M-Juno r2 motherboard.

This section contains the following subsections:

- *1.1.1 Ensuring safety* on page 1-12.
- *1.1.2 Preventing damage* on page 1-12.

1.1.1 Ensuring safety

An on-board connector supplies 12V DC to the V2M-Juno r2 motherboard.

Warning

Do not use the V2M-Juno r2 motherboard near equipment that is sensistive to electromagnetic emissions, for example, medical equipment.

1.1.2 Preventing damage

The V2M-Juno r2 motherboard is intended for use within a laboratory or engineering development environment. It is supplied with an enclosure that leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

Caution

To avoid damage to the V2M-Juno r2 motherboard, observe the following precautions:

- Connect the external power supply to the board before powerup to prevent damage.
- Never subject the board to high electrostatic potentials. Observe Electrostatic discharge (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Do not use the board near a transmitter of electromagnetic emissions.

1.2 About the Versatile™ Express Juno r2 Development Platform

The Juno r2 Development Platform, that is, the V2M-Juno r2 motherboard, is a development motherboard that provides access to the Juno r2 ARM Development Platform SoC. This is a development chip that supports ARMv8-A software tooling, evaluation, and development.

The V2M-Juno r2 motherboard provides the following:

Juno r2 ARM Development Platform SoC (Juno r2 SoC)

The Juno r2 SoC provides a fully coherent dual-core Cortex®-A72 cluster, a fully coherent quad-core Cortex-A53 cluster, and an I/O-coherent Mali™-T624 quad-core GPU cluster.

Dual-core Cortex-A72 cluster:
2MB L2 cache.
NEON™ and FPU.
Underdrive: Maximum operating frequency: 600MHz.
Nominal drive: Maximum operating frequency: 1GHz.
Overdrive: Maximum operating frequency: 1.2GHz.

Quad-core Cortex-A53 cluster:
1MB L2 cache.
NEON and FPU.
Underdrive: Maximum operating frequency: 450MHz.
Nominal drive: Maximum operating frequency: 800MHz.
Overdrive: Maximum operating frequency: 950MHz.

Quad-core Mali-T624 cluster:
1MB L2 cache.
NEON and FPU.
Underdrive: Maximum operating frequency: 450MHz.
Nominal drive: Maximum operating frequency: 600MHz.
Overdrive: Not supported.

Separate power domains support power management through *Dynamic Voltage and Frequency Scaling* (DVFS) of the Cortex-A72 and processor Cortex-A53 clusters, and the Mali-T624 GPU cluster.

Note

See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* for more information on the Juno r2 SoC.

LogicTile site

The V2M-Juno r2 motherboard provides two headers that enable you to fit a Versatile Express LogicTile daughterboard. A Thin Links TLX-400 Network Interconnect connects the motherboard and daughterboard.

Powerup and configuration system

An on-board EEPROM stores board and file identification information and a microSD card stores software images and configuration files. You can access the microSD card to perform configuration file editing and to update software images.

Configuration of the V2M-Juno r2 motherboard and the LogicTile daughterboard, if fitted, proceeds automatically under the control of the *Motherboard Configuration Controller* (MCC) after powerup or reset.

You can customize the clock speeds and other configuration settings.

IOFPGA

The IOFPGA provides low-bandwidth peripherals that the Juno r2 SoC does not provide. The IOFPGA connects to the Juno r2 SoC through a 32-bit *Static Memory Bus* (SMB) with dedicated chip selects.

The IOPFGA also contains energy meters, consisting of dedicated registers, that form part of the power control and DVFS system.

External user memory

8GB on-board DDR3L 800MHz connects to memory interfaces in the Juno r2 SoC. 64MB NOR flash connects to the IOFPGA. The IOFPGA contains 256KB of user RAM.

Access ports

The V2M-Juno r2 motherboard provides access through a general-purpose dual-UART, *Static Memory Controller* (SMC) 10/100 Ethernet port, four USB 2.0 ports, keyboard and mouse ports, Gen 2 PCI Express with four expansion slots, a Gigabit Ethernet port, and two SATA ports. The GbE port and SATA ports access the test chip through the PCI Express switch.

Video and audio output

The V2M-Juno r2 motherboard provides dual HDMI outputs. The Juno r2 SoC sends two independent 24-bit RGB video channels to the HDMI transmitters. Both HDMI ports share the same single I^2S audio from the Juno r2 SoC.

Additional user key entry

The V2M-Juno r2 motherboard supports trusted keyboard entry and additional key entry to simulate hand-held devices.

User LEDs

The V2M-Juno r2 motherboard provides eight user LEDs that connect to the IOFPGA. The meaning of each LED depends on the software that you implement in the Juno r2 SoC.

System LEDs

The V2M-Juno r2 motherboard provides LEDs that denote the status of the board power supplies. They also indicate the status of the read and write access to the configuration microSD card through the configuration USB port or configuration Ethernet port.

Debug

The V2M-Juno r2 motherboard supports P-JTAG processor debug that enables connection of DSTREAM, or a compatible third-party debugger. The board also supports 32-bit trace.

1.3 Location of components on the V2M-Juno r2 motherboard

The following figure shows the physical layout of the upper face of the V2M-Juno r2 motherboard.

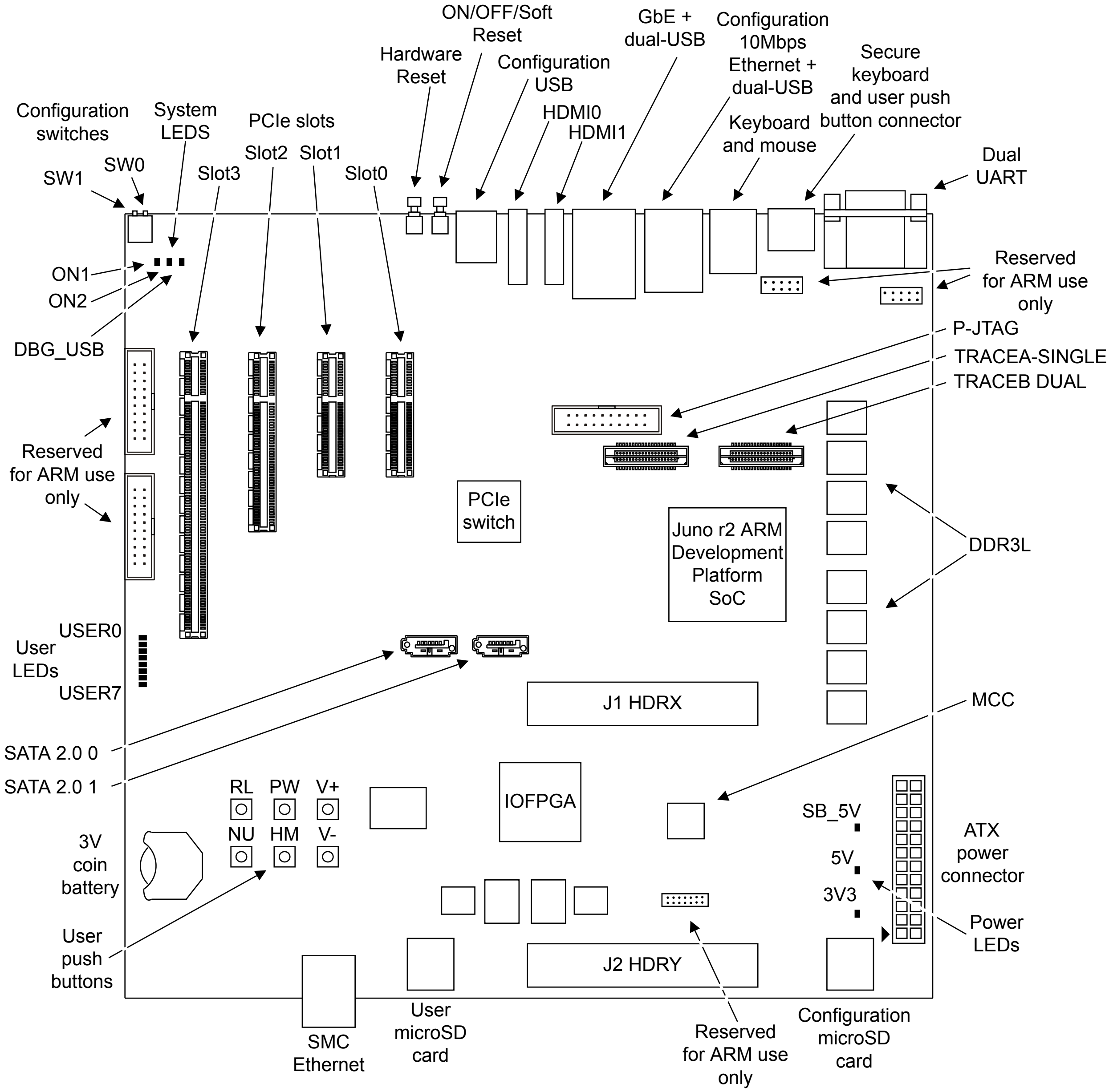


Figure 1-1 V2M-Juno r2 motherboard layout, upper face

1.4 Connectors on front and rear panels

The following figure shows the front panel of the case.

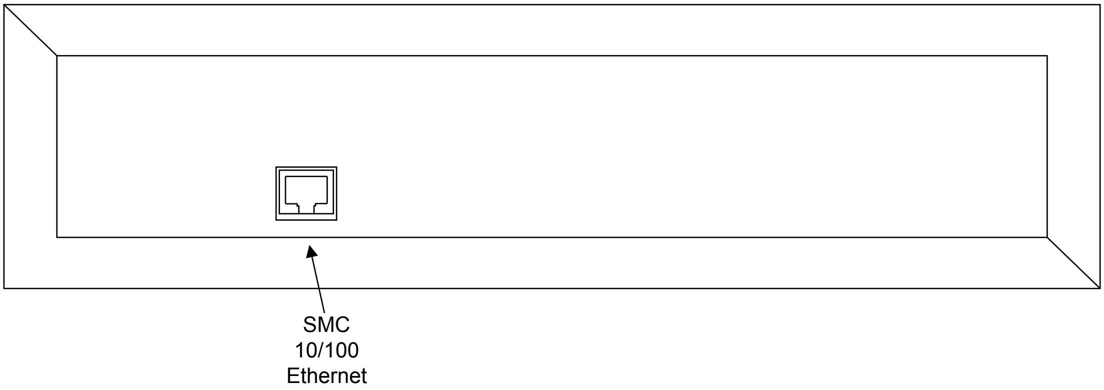


Figure 1-2 Front panel

The following figure shows the rear panel of the case.

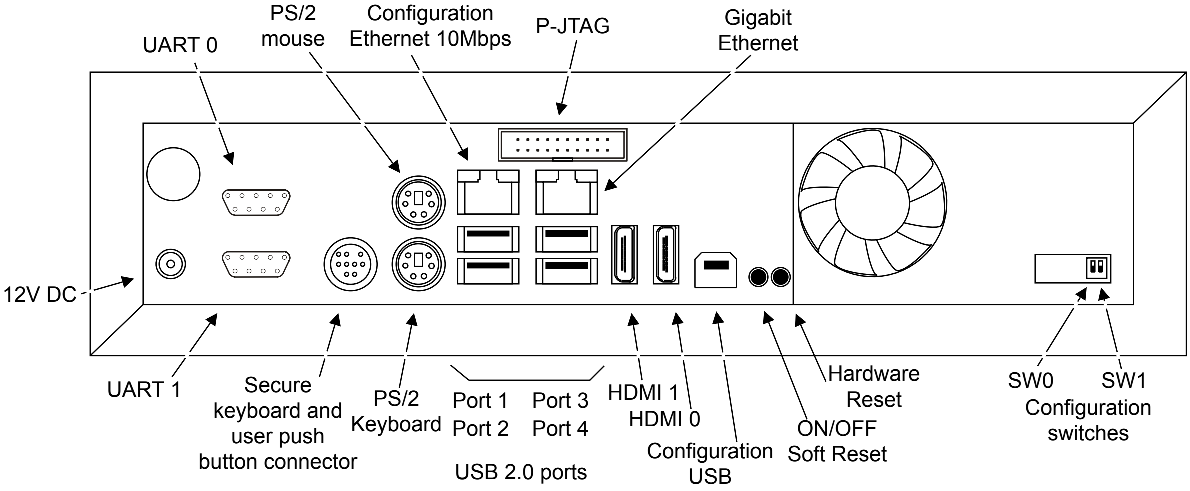


Figure 1-3 Rear panel

Chapter 2
Hardware Description

This chapter describes the Versatile Express V2M-Juno r2 motherboard hardware.

It contains the following sections:

2.1 Overview of V2M-Juno r2 motherboard hardware

The hardware infrastructure of the V2M-Juno r2 motherboard supports ARMv8-A software evaluation and tooling development using the Juno r2 SoC.

The following figure shows the hardware infrastructure of the V2M-Juno r2 motherboard.

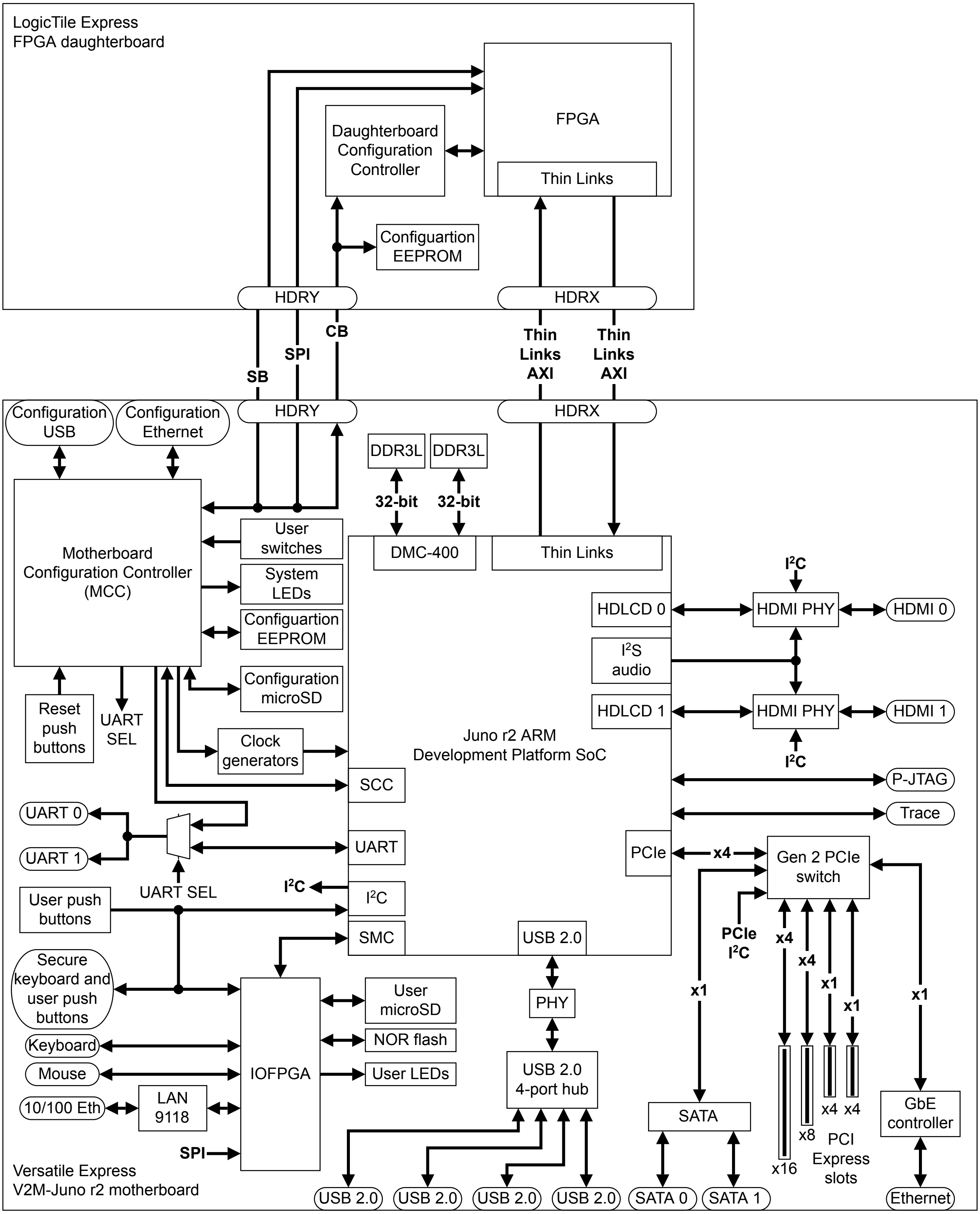


Figure 2-1 V2M-Juno r2 motherboard system architecture with LogicTile FPGA daughterboard

The V2M-Juno r2 motherboard contains the following components and interfaces:

- One Juno r2 SoC:
  - Dual-core Cortex-A72.
  - Quad-core Cortex-A53.
  - Quad-core Mali-T624 GPU.
  - Memory interfaces, HDLCD display controllers, PCIe root complex, and other on-chip peripherals.
- Site for LogicTile Express daughterboard:
  - Two headers, *HDRX* and *HDRY*, enable you to fit any Versatile Express LogicTile daughterboard in this site.
  - Thin Links AXI master and slave interfaces to LogicTile site.
- One Cortex-M3 *Motherboard Configuration Controller* (MCC) that supports configuration of the Juno r2 SoC and V2M-Juno r2 motherboard at powerup or reset:
  - Clock generator configuration.
  - Loading of *Real Time Clock* (RTC) registers.
  - Board configuration.
  - Pre-loading of external memory.
- One microSD card that stores the following:
  - Board configuration files.
  - Software images.
- One EEPROM that stores board identification information and file names for the configuration system.
- Configuration ports.

  The following ports support *Drag-and-Drop* editing of configuration files in the configuration microSD card:
  - Configuration USB 2.0 port.
  - Configuration 10Mbps Ethernet port.
- Two 32-bit 4GB DDR3L on-board memories:
  - Low-power.
  - 800MHz, 1600 million transfers per second (MTs).
- One PCI Express switch:
  - Provides connectivity to the SATA, 1000Base-T (Gbe) Ethernet, and PCIe expansion slots.
  - Four PCIe Gen 2 lanes to the Juno r2 SoC.
- Two SATA ports:
  - Connects to a Silicon Image Sil3232 SATA controller with a x1 Gen 1 connection to the PCIe switch.
  - Serial ATA Generation 2 transfer rate of 3.0 Gbps.
- Two 4-lane and two 1-lane PCIe Gen 2 expansion slots that connect directly to the PCIe switch.
- One 1000Base-T Ethernet port through PCIe that connects to a Marvell 88E8057-A0-NNB2C000 Gigabit Ethernet controller with a x1 connection to the PCIe switch.
- *Static Memory Controller* (SMC) 10/100 Ethernet port that uses a LAN9118 Ethernet controller.
- Four USB 2.0 ports, USB 4-port hub and USB PHY.
- Two UARTs:
  - UART 0 can connect to the Juno r2 SoC or to the MCC.
  - UART 1 can connect to the Juno r2 SoC or to the Daughterboard Configuration Controller on the LogicTile daughterboard fitted in the daughterboard site.

    The board configuration files, that you can edit using the configuration ports, determine the connectivity of the UART ports during runtime.

    Note

    The Daughterboard Configuration Controller is a microcontroller on the LogicTile that controls the configuration of the daughterboard during powerup or reset.

- Two HDLCD ports that each support:
  - — HDMI 1.4a up to 1080p.
  - — One I^2S four-channel stereo audio output.
- Additional user key entry:
  - — Trusted user keyboard entry using the secure keyboard connector.
  - — Additional user key entry using the push buttons on the V2M-Juno r2 motherboard to simulate hand-held devices.
- IOFPGA that contains the following:
  - — Registers that form part of the Power Control and DVFS system.
  - — SBCon controllers that configure the PCIe switch, the PCIe clock, and the HDMI PHYs.

  The IOFPGA also provides access to the following low-bandwidth peripherals, user switches, and user LEDs that the Juno r2 SoC does not provide:
  - — 64MB NOR flash.
  - — 256KB IOFPGA internal block RAM.
  - — User microSD card slot.
  - — Keyboard and mouse ports.
  - — Six user push buttons for additional user key entry.
  - — System registers.
  - — Current, voltage, power, and energy meters.
  - — Timers.
  - — Eight user LEDs. Application software defines their meaning.
- On-board clocks that generate source clocks for Juno r2 SoC and V2M-Juno r2 motherboard systems.
- A real-time clock in the MCC. A 3V coin battery powers the real-time clock when the board is powered down.
- Three system LEDs that connect to the MCC as follows:

  ON1 LED:
    Reserved for ARM use only.

  ON2 LED:
    Denotes ATX power supply powered up.

  Debug USB LED:
    Denotes read or write access to the configuration microSD card through the configuration USB 2.0 port.
- Debug ports:
  - — 32-bit CoreSight Trace port.
  - — Processor CoreSight debug (P-JTAG) port.

2.2 Juno r2 ARM Development Platform SoC

The Juno r2 SoC development chip provides a dual-core Cortex-A72 cluster, a quad-core Cortex-A53 cluster, a quad-core Mali-T624 graphics cluster, interfaces, on-chip peripherals, and internal network connect.

The following figure shows the architecture of the Juno r2 SoC.

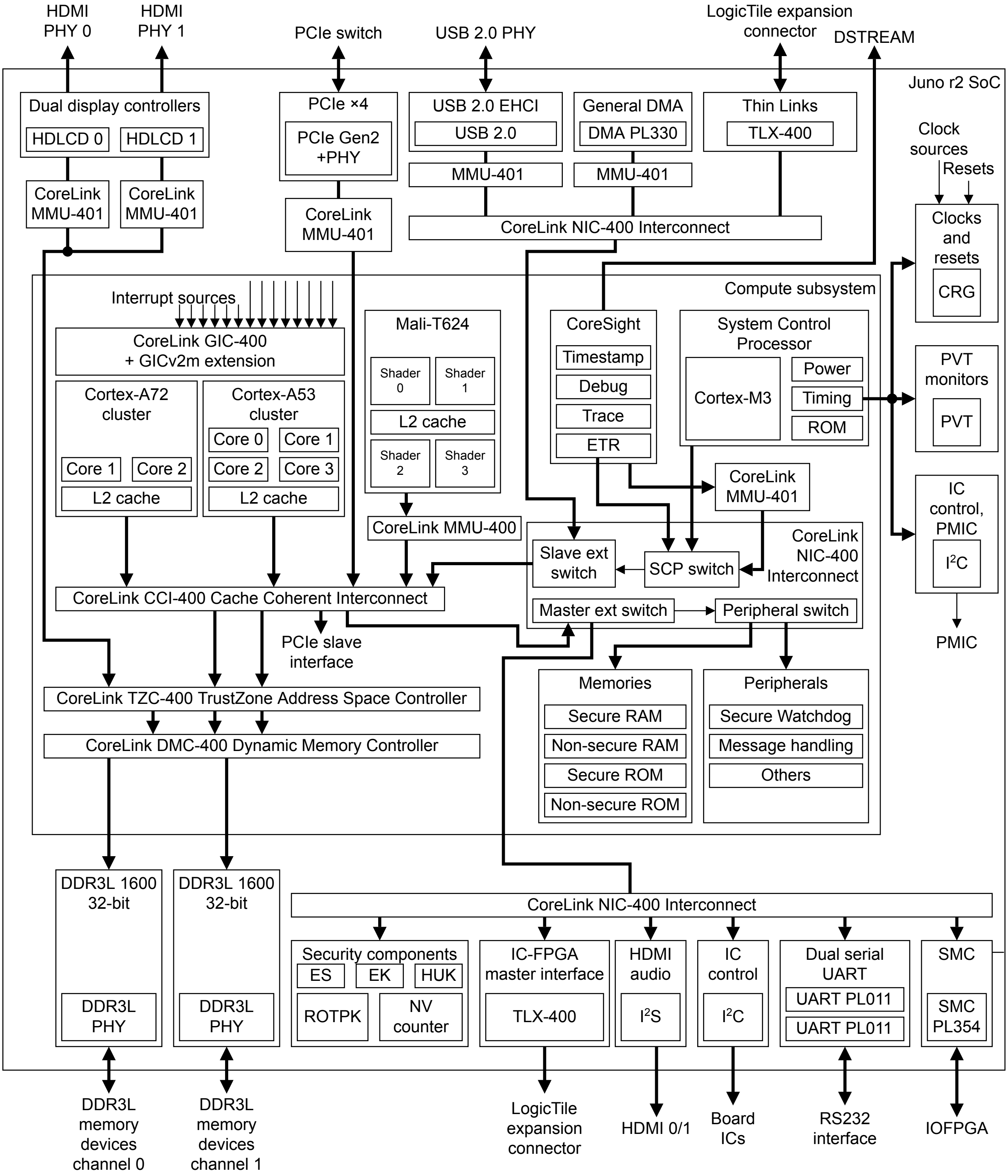


Figure 2-2 Architecture of the Juno r2 SoC

The Juno r2 SoC contains the following components and interfaces:

- Dual-core Cortex-A72 cluster:
  - — 2MB L2 cache.
  - — NEON and *Floating Point Unit* (FPU).
  - — Underdrive: Maximum operating frequency: 600MHz.

  - Nominal drive: Maximum operating frequency: 1GHz.
  - Overdrive: Maximum operating frequency: 1.2GHz.
- Quad-core Cortex-A53 cluster:
  - 1MB L2 cache.
  - NEON and FPU.
  - Underdrive: Maximum operating frequency: 450MHz.
  - Nominal drive: Maximum operating frequency: 800MHz.
  - Overdrive: Maximum operating frequency: 950MHz.
- Mali-T624 quad-core GPU cluster:
  - Underdrive: Maximum operating frequency: 450MHz.
  - Nominal drive: Maximum operating frequency: 600MHz.
  - Overdrive: Not supported.
- Internal AXI subsystem operating at up to 533MHz.
- Dual ARM HDLCD display controllers that support HDMI 1.4a up to 1080p.
- Dual DDR3L PHY and 32-bit DDR3L interfaces.
- PCIe Gen 2 4-lane root complex and PHY with coherent and non-coherent modes.
- Thin Links AXI master and slave interfaces to the LogicTile site. At the default clock frequency of 61.5MHz, the operating bit rates are:
  - Master interface: 68Mbps in the forward direction and 78Mbps in the reverse direction.
  - Slave interface: 246Mbps in the forward direction and 305Mbps in the reverse direction.

  Note

  The forward direction is from master to slave and the reverse direction is from slave to master.

- USB 2.0 host controller. This is a 480Mbps ULPI interface to off-chip PHY.
- PL354 *Static Memory Controller* (SMC).
- PL330 *Direct Memory Access* (DMA) controller.
- CoreSight processor debug (P-JTAG) and trace.
- APB subsystem:
  - Dual-UART.
  - I^{2}S 4-channel stereo audio.
  - *Power, Voltage, and Temperature* (PVT) monitoring of Juno r2 ARM Development Platform SoC.
  - Non-volatile counter. A real time clock that retains its stored value after powerdown.
  - *System Control Processor* (SCP). This is a Cortex-M3 processor integrated into the Juno r2 SoC. It initiates the system architecture and pre-loads memory at powerup and performs power management and system control functions during runtime.
  - I^{2}C. This connects to HDMI controllers, the UART transceiver, and other components on the V2M-Juno r2 motherboard.
  - Secure I^{2}C. This connects to the secure keyboard.
  - Keys. Encryption keys for signing software.
  - Random-number generator. This operates with the encryption keys when validating software.
  - System override registers that enable you to override various aspects of the Juno r2 SoC.

See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* for more information. This document lists, in the *Additional Reading* section, references to ARM IP, such as the PL011 for example, inside the Juno r2 SoC.

2.3 External power

The mains supply powers the V2M-Juno r2 motherboard using the on-board connector, an external power supply unit, and a connector cable that ARM supplies with the V2M-Juno r2 motherboard.

The external power supply unit converts mains power to 12V DC and this connects to the 12V DC connector on the rear panel of the case. The unit accepts mains power in the range 100-240V AC.

Alternatively, you can connect an ATX power supply unit directly to the board.

On-board regulators supply power to the V2M-Juno r2 motherboard power domains and to the power domains of the Juno r2 SoC.

Power LEDs indicate the power domains that are active:

5V	5V domain powered.
3V3	3V3 domain powered.
SB_5V	Standby 5V domain powered.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.13 ATX power connector on page Appx-A-145.

2.4 Power management and temperature protection

The Juno r2 SoC provides internal power management and monitoring, and over-temperature protection.

This section contains the following subsections:

- *2.4.1 Power control and Dynamic Voltage and Frequency Scaling (DVFS)* on page 2-26.
- *2.4.2 PVT sensor* on page 2-27.

2.4.1 Power control and Dynamic Voltage and Frequency Scaling (DVFS)

The V2M-Juno r2 motherboard provides DVFS, in addition to monitoring the voltage, current, power, temperature, and energy consumption of the Juno r2 SoC power domains.

The V2M-Juno r2 motherboard contains a *Power Management IC* (PMIC) that generates the V2M-Juno r2 motherboard and Juno r2 SoC power supplies. The Juno r2 SoC configures the PMIC through the *System Control Processor* (SCP) I^2C interface during powerup or reset.

Direct control of the PMIC through the SCP interface during runtime supports voltage scaling.

Varying the Juno r2 SoC PLL dividers during runtime supports frequency scaling.

Note

ARM recommends that you use this method to achieve frequency scaling and do not use external control of the clock generators through the V2M-Juno r2 motherboard SCP I^2C interface.

Dedicated logic blocks in the IOFPGA contain current, voltage, power, and energy meters for the Cortex-A53, Cortex-A72, Mali-T624 GPU, and VSYS supplies. These register addresses are in the APB Registers memory space.

Note

The VSYS supply powers the fabric of the Juno r2 SoC outside the Cortex-A53, Cortex-A72, and Mali-T624 GPU clusters.

The following figure shows the V2M-Juno r2 motherboard power control and DVFS system.

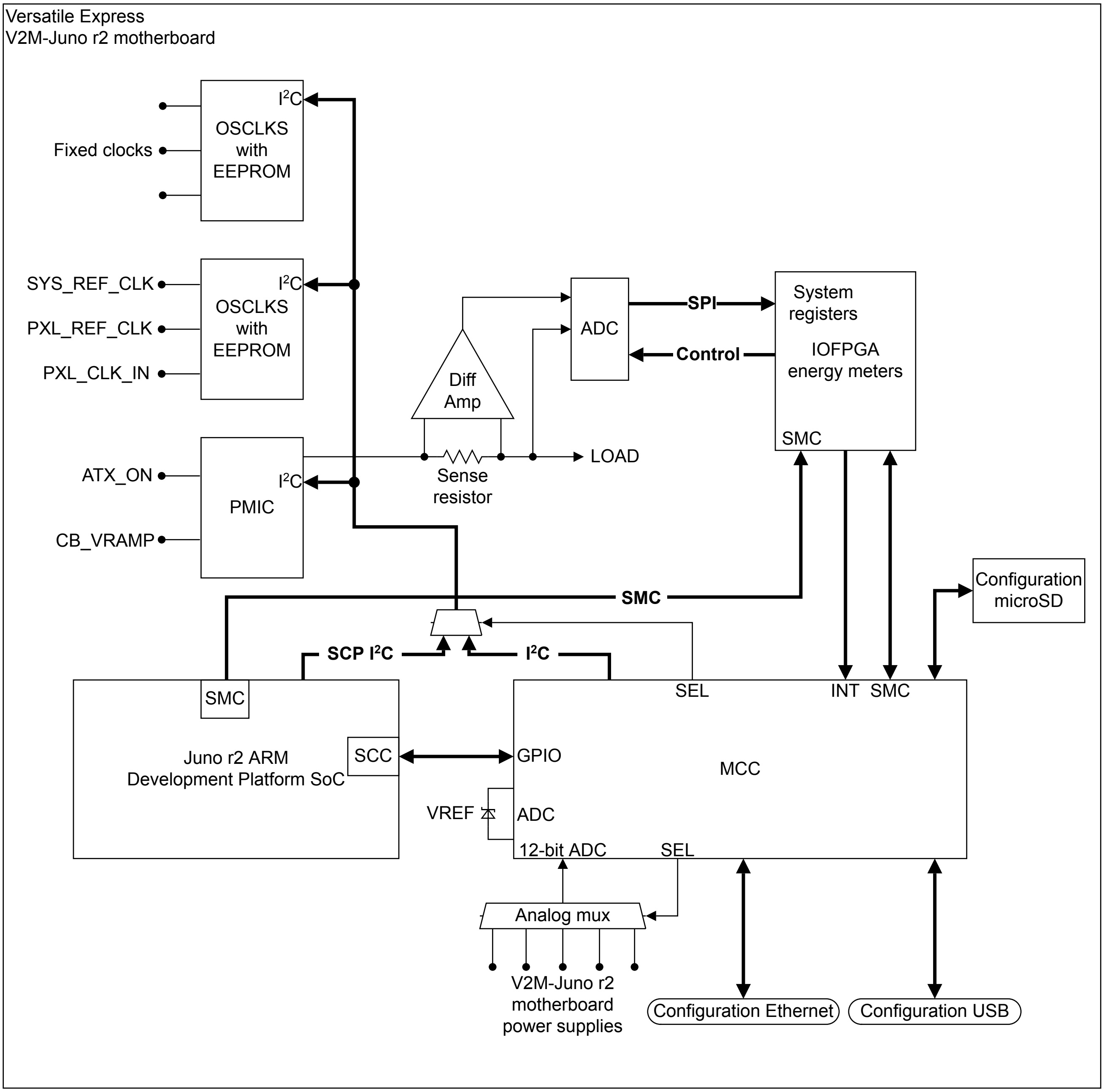


Figure 2-3 Power control and DVFS system

Related concepts

4.5.1 APB energy register summary on page 4-106.

2.4.2 PVT sensor

The Juno r2 SoC provides a *Power, Voltage, and Temperature* (PVT) sensor that powers down the chip when it exceeds the maximum operating temperature. It also selectively powers down parts of the chip when it exceeds the temperature budget.

The PVT sensor is calibrated during board manufacture.

2.5 Clocks

V2M-Juno r2 motherboard clocks drive the board, the Juno r2 SoC, and the LogicTile, if fitted in the daughterboard site.

This section contains the following subsections:
- *2.5.1 Overview of clocks* on page 2-28.
- *2.5.2 Juno r2 SoC and V2M-Juno r2 motherboard clocks* on page 2-28.
- *2.5.3 IOFPGA clocks* on page 2-32.

2.5.1 Overview of clocks

Clock generators on the V2M-Juno r2 motherboard generate clocks for the internal blocks in the Juno r2 SoC, the internal blocks in the IOFPGA, and the peripherals on the board.

During powerup or reset, internal EEPROMs in the clock generators configure the generators to the correct operational clock frequencies. The `board.txt` file also defines these default clock frequencies. You can change the operational clock frequencies by modifying the configuration `board.txt` file.

Note

ARM recommends that you operate the V2M-Juno r2 motherboard at the default clock frequencies.

Related concepts

3.3.3 Contents of the `MB` directory on page 3-72.

2.5.2 Juno r2 SoC and V2M-Juno r2 motherboard clocks

The following figure shows the Juno r2 SoC clocks and clock domains. The figure includes the clocks that connect to the LogicTile Express daughterboard, to some of the peripherals on the V2M-Juno r2 motherboard, and to the IOFPGA.

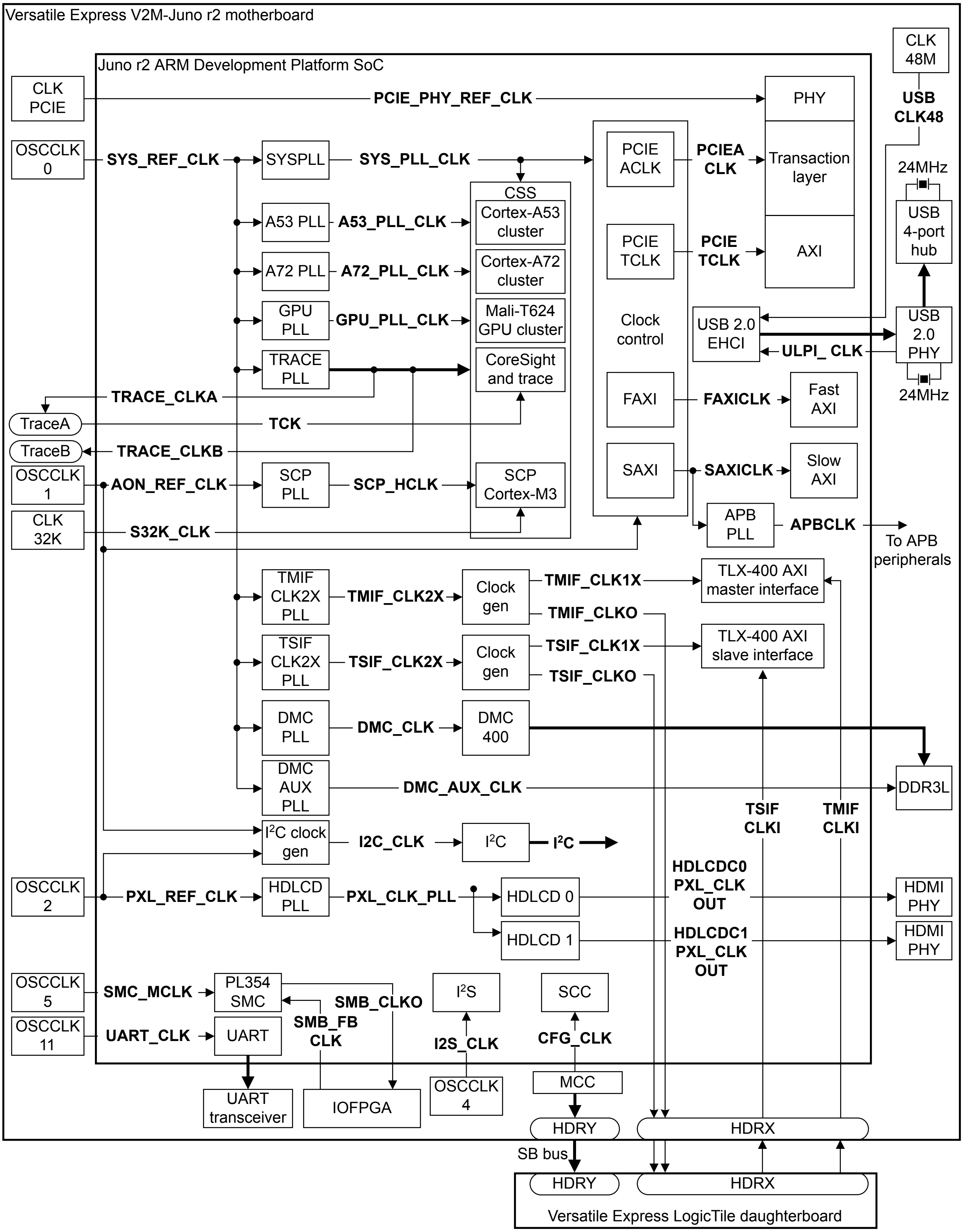


Figure 2-4 Juno r2 SoC system clocks

The following table shows the internal Juno r2 SoC and V2M-Juno r2 motherboard clocks and their sources.

Table 2-1 Juno r2 SoC clocks and their sources on the V2M-Juno r2 motherboard

Juno r2 SoC clock	Source	Juno r2 SoC clock default frequency	Description
SYS_REF_CLK	OSCCLK 0	50MHz	Main system clock for the Juno r2 SoC. Source clock for the following systems and PLLs inside the Juno r2 SoC: **CSS main system clock:** 1600MHz. **Cortex-A72 clock (A72_PLL_CLK) maximum operating frequencies:** Underdrive: 600MHz. Nominal: 1GHz. Overdrive: 1.2GHz. **Cortex-A53 clock (A53_PLL_CLK) maximum operating frequencies:** Underdrive: 450MHz. Nominal: 800MHz Overdrive: 950MHz. **Mali-T624 GPU clock (GPU_PLL_CLK) maximum operating frequencies:** Underdrive: 450MHz. Nominal: 600MHz. Overdrive: Not supported. **DMCCLK**: DMC-400 clock. 400MHz. **DMC_AUX_CLK**: External DMC interface on V2M-Juno r2 motherboard clock. 800MHz. **FAXICLK**: Fast AXI clock. 533MHz. **SAXICLK**: Slow AXI clock. 400MHz. **PCIEA_CLK** 133MHz Transaction layer clock in the PCI Express Root Complex. **PCIE_TCLK** 133MHz Clocks the AXI logic associated with the PCI Express Root Complex. **USBHCLK**: Primary clock for the BIU of the USB EHCI and OHCI host controllers. 160MHz. **TMIF_CLK2X**: AXI master interface reference clock in the forward direction. 123MHz. **TSIF_CLK2X**: AXI slave interface reference clock in the reverse direction. 123MHz. **APBCLK**: Clocks the SMB_CLK domain in the IOFPGA. 100MHz. **TRACE_CLKA, TRACE_CLKB**: 145.45MHz.
AON_REF_CLK	OSCCLK 1	50MHz	Source clock for the I^2C clock generator and reference clock for the SCP PLL inside the Juno r2 SoC. This derives the following clock: **SCPHCLK**: SCP subsystem and AHB expansion area clock.

Table 2-1 Juno r2 SoC clocks and their sources on the V2M-Juno r2 motherboard (continued)

Juno r2 SoC clock	Source	Juno r2 SoC clock default frequency	Description
PXL_REF_CLK	OSCCLK 2	50MHz	Reference clock for the HDLCD PLL inside the Juno r2 SoC. This generates **PXL_PLL_CLK**, 23.75MHz.
HDLCDC0_PXL_CLK_OUT	HDLCD0 in Juno r2 SoC	165MHz	Pixel clock to HDMI PHY 0 on the V2M-Juno r2 motherboard. The default operating frequency of the PHY, 165MHz, is also the maximum operating frequency.
HDLCDC1_PXL_CLK_OUT	HDLCD1 in Juno r2 SoC	165MHz	Pixel clock to HDMI PHY 1 on the V2M-Juno r2 motherboard. The default operating frequency of the PHY, 165MHz, is also the maximum operating frequency.
S32K_CLK	CLK_32K clock generator	32.768kHz	Fixed frequency real-time clock. Provides a real-time private time domain for the SCP that uses it to implement very low-power sleep modes.
I2S_CLK	OSCCLK 4	2.11MHz	Integrated-IC sound clock. Clocks the I^2S audio bus.
I2C_CLK	OSCCLK 1	50MHz	Clocks the I^2C control bus.
UART_CLK	OSCCLK 11	7.3728MHz	Clocks the UART interface.
TCK	Trace connector	25MHz	From external trace port analyzer. Clocks the Trace debug system.
ULPI_CLK	USB2 2.0 xtal clock generator	60MHz	Fixed frequency clock. Clocks the *USB 2.0 Transceiver Macrocell Interface Low-Pin Interface* (ULPI) from the off-chip PHY.
USB_CLK48	CLK_48M clock generator	48MHz	Primary clock input to the USB controller.
PCIE_PHY_REF_CLK	CLK_PCIE clock generator	125MHz	Fixed frequency differential clock. PCIe reference clock.
SMC_MCLK	OSCLK 5	50MHz	Clocks the PL354 *Static Memory Controller* (SMC) interface.
SMC_FB_CLK	IOFPGA	50MHz	Feedback clock from IOFPGA to read data back into the PL354 in synchronous mode. The SMC uses this to adjust timing.
SMC_CLKO	OSCLK 5	50MHz	Derived from **SMC_MCLK**. Exported from Juno r2 SoC to the SMB timing adjust block in the IOFPGA.
CFG_CLK	MCC	10MHz	*Serial Configuration Controller* (SCC) serial interface clock.
TMIF_CLKI	TLX-400 Thin Links AXI slave interface in FPGA on LogicTile fitted in daughterboard site	61.5MHz	Clock in the receive direction to the TLX-400 Thin Links AXI master interface on the Juno r2 SoC.
TMIF_CLKO	TLX-400 Thin Links AXI master interface reference clock generator in Juno r2 SoC	61.5MHz	Clock in the transmit direction from the TLX-400 Thin Links AXI master interface on the Juno r2 SoC.

Table 2-1 Juno r2 SoC clocks and their sources on the V2M-Juno r2 motherboard (continued)

Juno r2 SoC clock	Source	Juno r2 SoC clock default frequency	Description
TSIF_CLKI	TLX-400 Thin Links AXI master interface in FPGA on LogicTile fitted in daughterboard site	61.5MHz	Clock in the receive direction to the TLX-400 Thin Links AXI slave interface on the Juno r2 SoC.
TSIF_CLKO	TLX-400 Thin Links AXI slave interface reference clock generator in Juno r2 SoC	61.5MHz	Clock in the transmit direction from the TLX-400 Thin Links AXI slave interface on the Juno r2 SoC.

The MCC uses the `board.txt` configuration file in the microSD card to set the frequency of the board clock generators. You can adjust these default clock frequencies by editing this file. You can also adjust the board clocks during runtime by using the SYS_CFG register interface.

The Juno r2 SoC has internal PLLs and clock generators that generate clocks to drive the Juno r2 SoC internal systems.

2.5.3 IOFPGA clocks

The following figure shows the IOFPFA clocks and clock domains.

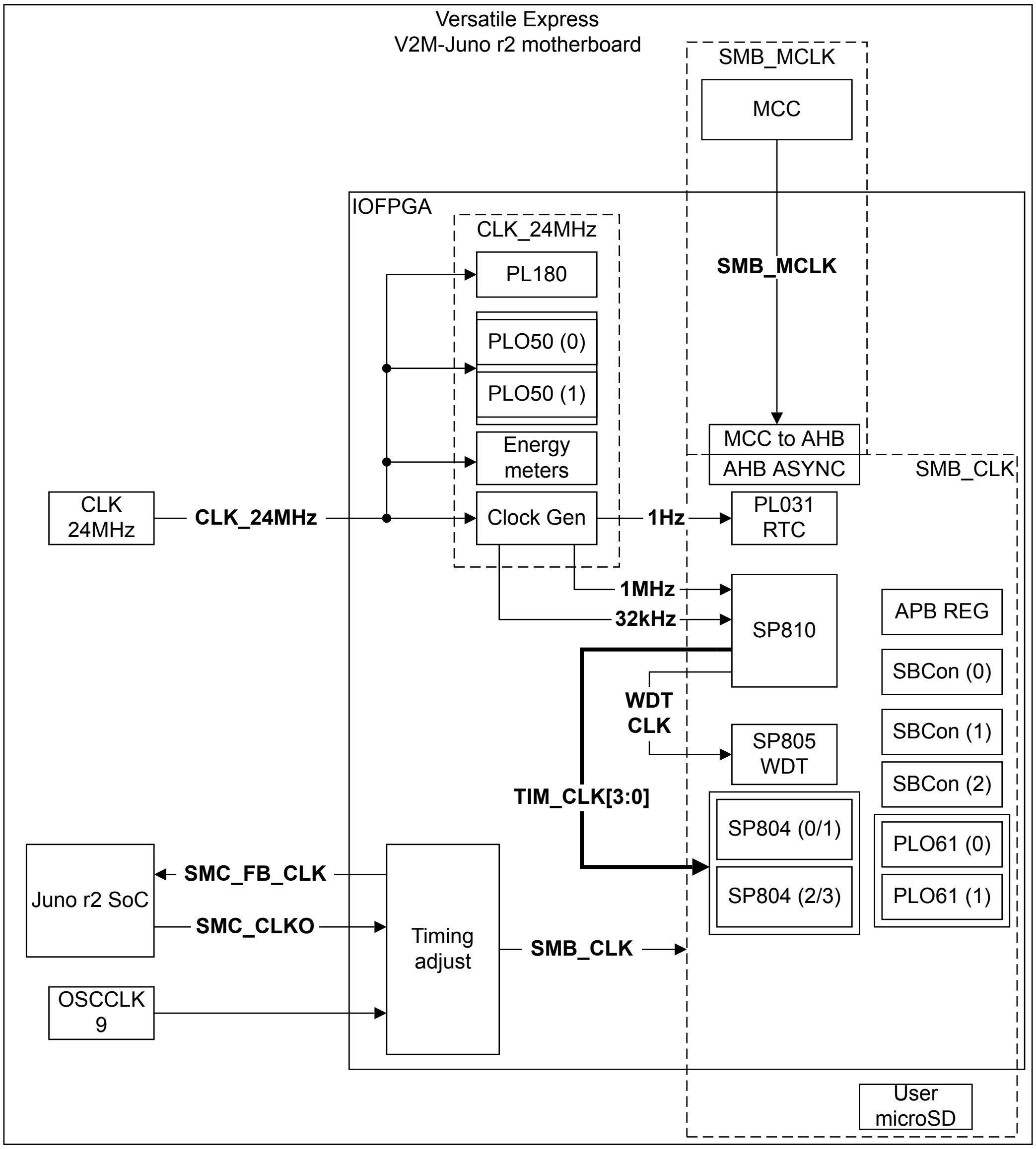


Figure 2-5 IOFPGA clocks

The bootup clock for the peripherals in the *SMB_CLK* domain during powerup and configuration is *OSCCLK 9* on the V2M-Juno r2 motherboard. The clock source then switches to **SMB_CLKO** from the Juno r2 SoC that becomes the master clock for the *SMB_CLK* domain during runtime.

Table 2-2 V2M-Juno r2 motherboard OSCCLK clock sources

Clock name	Source	Default Frequency	Description
SMB_CLK	OSCCLK 9 during powerup and configuration. **SMC_CLKO** during runtime.	50MHz	Reference clock for the *SMB_CLK* domain. This domain contains the following IOFPGA peripherals and subsystems: • AHB subsystem. • APB subsystem. • PL031 Real-Time Clock. • APB system registers. • System Bus Controllers, SBCon, that configure the PCIe switch, the HDMI PHYSs, and prepare the PCIe clock for configuration by the Juno r2 SoC. • SP805 Watchdog Timer. • SP804 Dual-Timers. • PL061 GPIO. • SP810 System Controller.
CLK_24MHZ	CLK_24MHZ clock generator.	24MHz fixed frequency	Reference clock for the following blocks inside the *SMB_CLK* clock domain: • PL180 MultiMedia Card Interface. • PL050 keyboard and mouse interfaces. • Energy meters, that is, the voltage, current, power, and accumulated energy meters. • The clock generator that generates the **32kHz** and **1MHz** source clocks for the SP810 System Controller and the **1Hz** clock for the PL031 Real-Time Clock. **Note** • The SP810 System Controller selects **32kHz** or **1MHz** as the sources for **TIM_CLK[3:0]**, the SP804 timer clocks. The powerup default is **32kHz**. It also generates the SP805 clock, **WDT_CLK**. • The frequency of the clock **32kHz** is 32.768kHz.
SMB_MCLK	MCC	50MHz	Master clock for the *SMB_MCLK* domain that includes the MCC, and the MCC to AHB fabric, in the IOFPGA.

2.6 Resets

The V2M-Juno r2 motherboard provides two reset push buttons and a reset system that control the reset timing sequence of the board.

This section contains the following subsections:

- *2.6.1 Reset push buttons* on page 2-35.
- *2.6.2 Reset architecture* on page 2-35.
- *2.6.3 Reset sequence* on page 2-37.

2.6.1 Reset push buttons

The V2M-Juno r2 motherboard provides the following reset push buttons.

Hardware Reset push button

Pressing the *Hardware Reset* button during runtime generates **nPBRESET**, that performs a hardware reset, and puts the system into standby state.

Note

The *Hardware Reset* push button is the black push button. The V2M-Juno r2 motherboard labels it as *nPBRESET*.

ON/OFF/Soft Reset push button

Pressing the *ON/OFF/Soft Reset* button:

- Briefly during runtime performs a software reset of the system.
- For more than two seconds puts the system into the standby state in the same way as pressing the *Hardware Reset* button.

Note

The *ON/OFF/Soft Reset* push button is the red push button. The V2M-Juno r2 motherboard labels it as *nPBON*.

When you use the system with bare metal software, you must make the following setting in the `config.txt` file to enable direct control of the OFF/Soft Reset feature:

```
PBONFORCE: TRUE     ;RED PBON push button directly drives RESET/SHUTDOWN
```

Related concepts

3.5.1 Use of ON/OFF/Soft Reset button on page 3-77.

3.5.2 Use of Hardware Reset button on page 3-77.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

2.6.2 Reset architecture

The following figure shows an overview of the V2M-Juno r2 motherboard reset system.

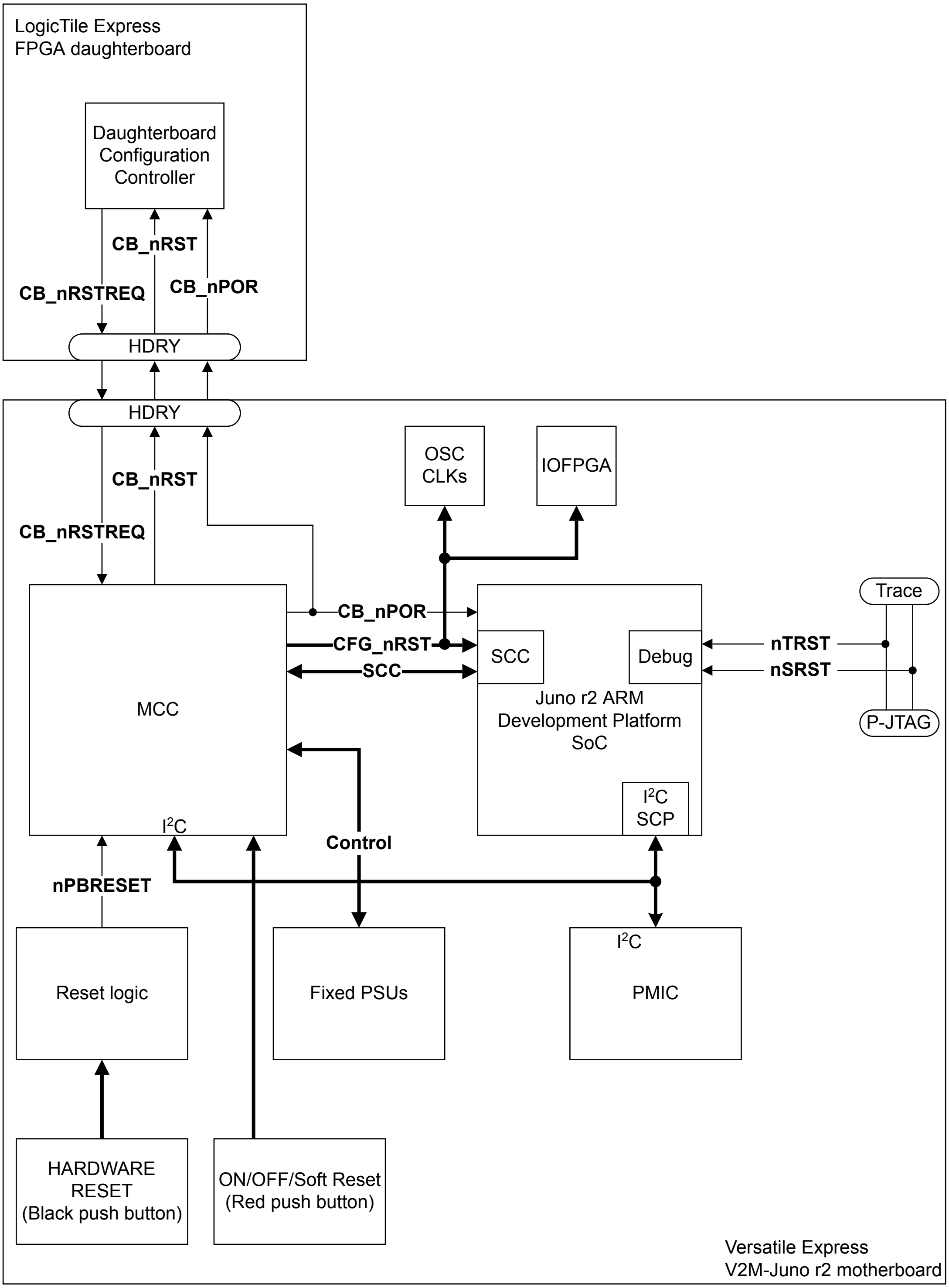


Figure 2-6 V2M-Juno r2 motherboard resets

CB_nPOR

This is the main powerup reset for the Juno r2 ARM Development Platform SoC, and the devices and peripherals on the V2M-Juno r2 motherboard including the IOFPGA. The **CB_nPOR** signal drives the **nPORESET** signal inside the Juno r2 SoC.

nTRST

This resets the CoreSight DAP and the TAP controllers inside the Juno r2 SoC.

CFG_nRST

This is the reset signal for the serial interface to the SCC registers in the Juno r2 SoC. It resets the SCC registers to their default values. It also resets the IOFPGA peripherals and the clock generators on the V2M-Juno r2 motherboard.

2.6.3 Reset sequence

The following figure shows the reset and configuration timing sequence.

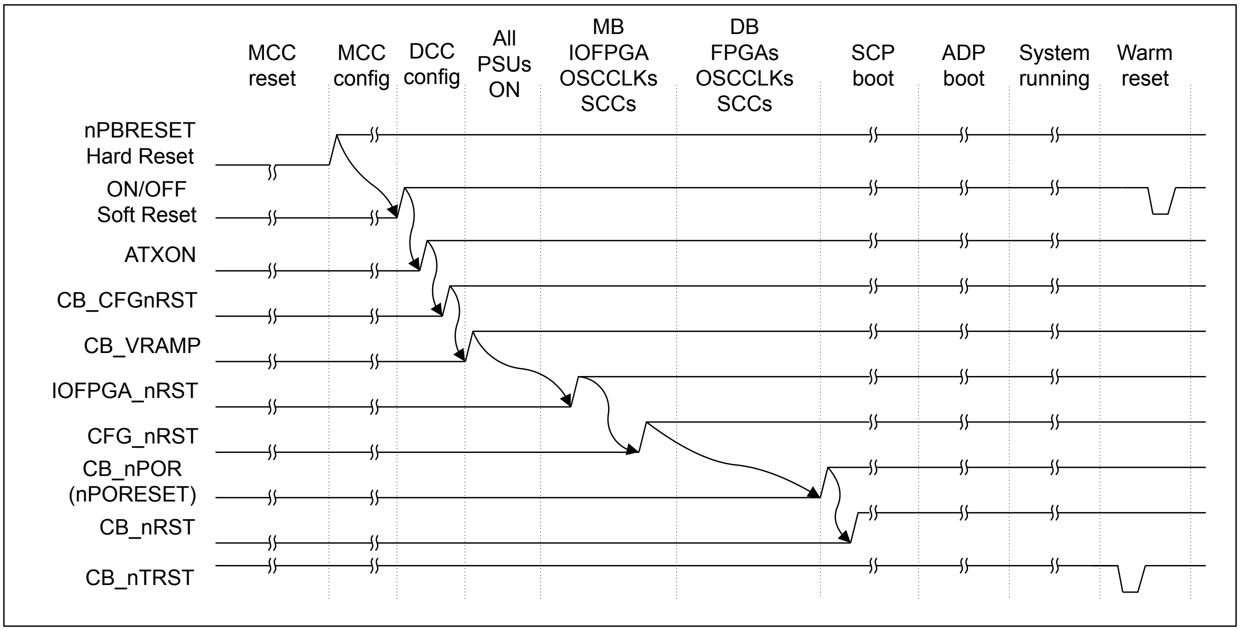


Figure 2-7 V2M-Juno r2 motherboard reset and configuration timing cycle

2.7 Thin Links

Thin Links master and slave interfaces connect the Juno r2 SoC to the daughterboard through the motherboard tile site.

This section contains the following subsections:

- *2.7.1 Overview of Thin Links master and slave interfaces* on page 2-38.
- *2.7.2 Thin Links master interface* on page 2-39.
- *2.7.3 Thin Links slave interface in non-coherent mode* on page 2-40.
- *2.7.4 Thin Links slave interface in coherent mode* on page 2-41.

2.7.1 Overview of Thin Links master and slave interfaces

The Juno r2 SoC contains one AXI master interface and one slave interface, that you can use in either coherent or non-coherent mode, that connect to the FPGA in the LogicTile Express daughterboard fitted in the V2M-Juno r2 motherboard tile site. A Thin Links TLX-400 interface compresses the master and slave interfaces to reduce the pin count.

The width of the TLX-400 slave interface on the Juno r2 SoC is greater than the width of the master interface.

The Thin Links ACE slave interface uses the same pins as the Thin Links AXI slave interface and enables the connection of a cache-coherent component to the V2M-Juno r2 motherboard tile site. The ACE slave interface is intended to be used in conjunction with the Thin Links AXI master interface. When the Thin Links ACE slave interface is in use, one of the Juno r2 SoC clusters is disabled.

The default Thin Links clock frequency of 61.5MHz gives the following operating speeds:

- Juno r2 SoC master interface:
  - — Forward direction, that is, from the Juno r2 SoC to the FPGA: 68Mbps.
  - — Reverse direction, that is, from the FPGA to the Juno r2 SoC: 78Mbps.
- Juno r2 SoC slave interface:
  - — Forward direction, that is, from the FPGA to the Juno r2 SoC: 246Mbps.
  - — Reverse direction, that is, from the Juno r2 SoC to the FPGA: 305Mbps.

Note

ARM recommends that you operate the Thin Links interfaces at the default speeds. See *3.3.4 Contents of the `SITE1` directory* on page 3-73 for an example `board.txt` configuration file that sets the Thin Links clocks to 61.5MHz.

The following table shows the Thin Links timing requirements.

Table 2-3 Thin Links timing requirements

Symbol	Min	Max	Description
Tsu	1.2ns	-	Input data parameter. Minimum data setup time before clock edge.
Th	1.0ns	-	Input data parameter. Minimum data hold time after clock edge.
Tcomin	-2.5ns	-	Tcomin is relative to clock edge. Data is available on the bus between Tcomin and Tcomax.
Tcomax	2.5ns	-	Tcomax is relative to clock edge. Data is available on the bus between Tcomin and Tcomax.

Note

Any Versatile Express LogicTile daughterboard fitted in the tile site that implements an ARM application note meets these timing requirements.

Any design that you implement in a Versatile Express LogicTile daughterboard, or in your own daughterboard, must meet these timing requirements.

2.7.2 Thin Links master interface

The following figure shows the Thin Links TLX-400 master interface on the Juno r2 SoC and its connection to the Thin Links TLX-400 slave interface on the LogicTile Express daughterboard.

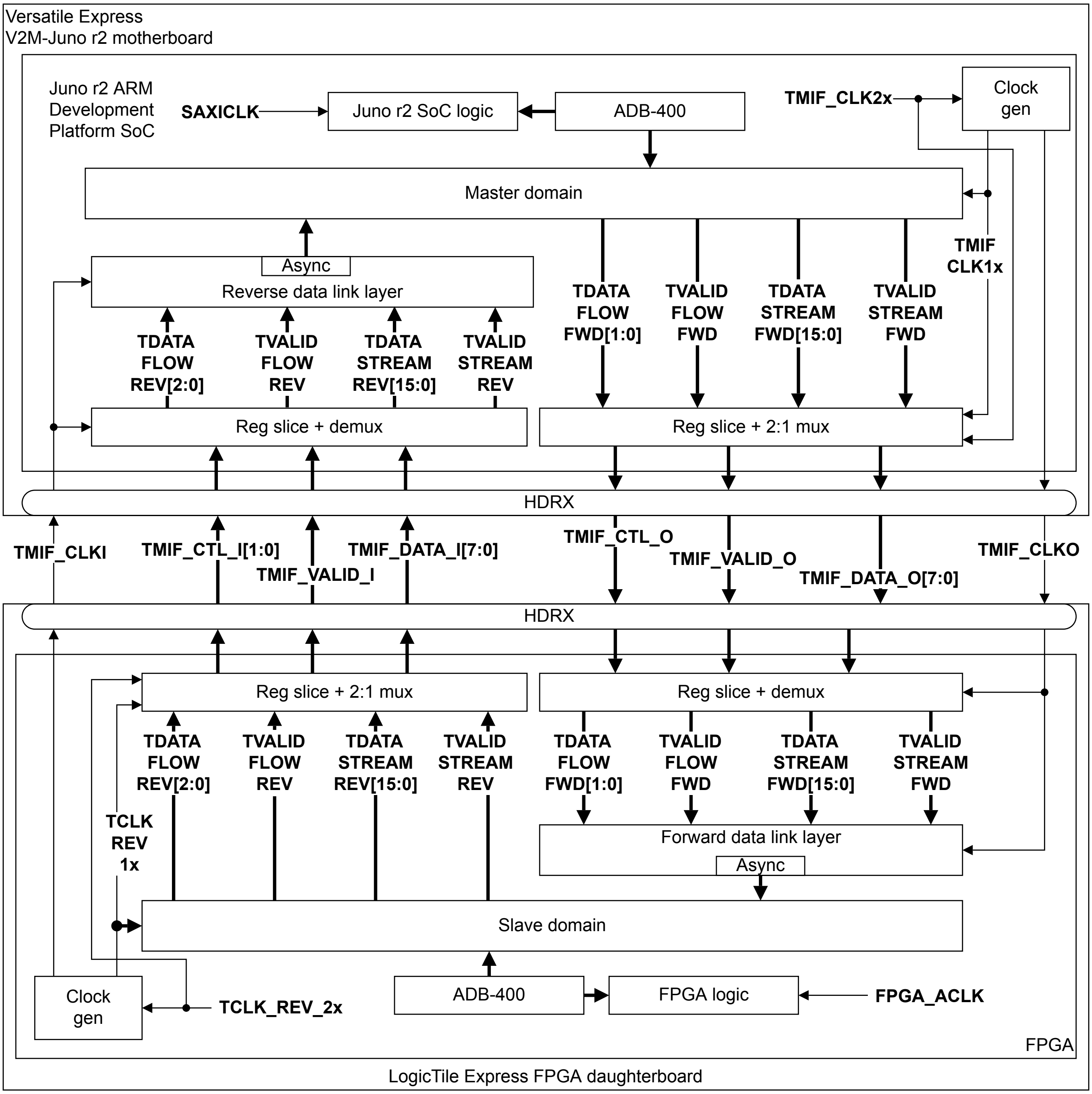


Figure 2-8 Thin Links AXI master interface

2.7.3 Thin Links slave interface in non-coherent mode

The following figure shows the Thin Links TLX-400 AXI slave interface on the Juno r2 SoC, that is the slave interface in non-coherent mode, and its connection to the Thin Links TLX-400 master interface on the LogicTile daughterboard.

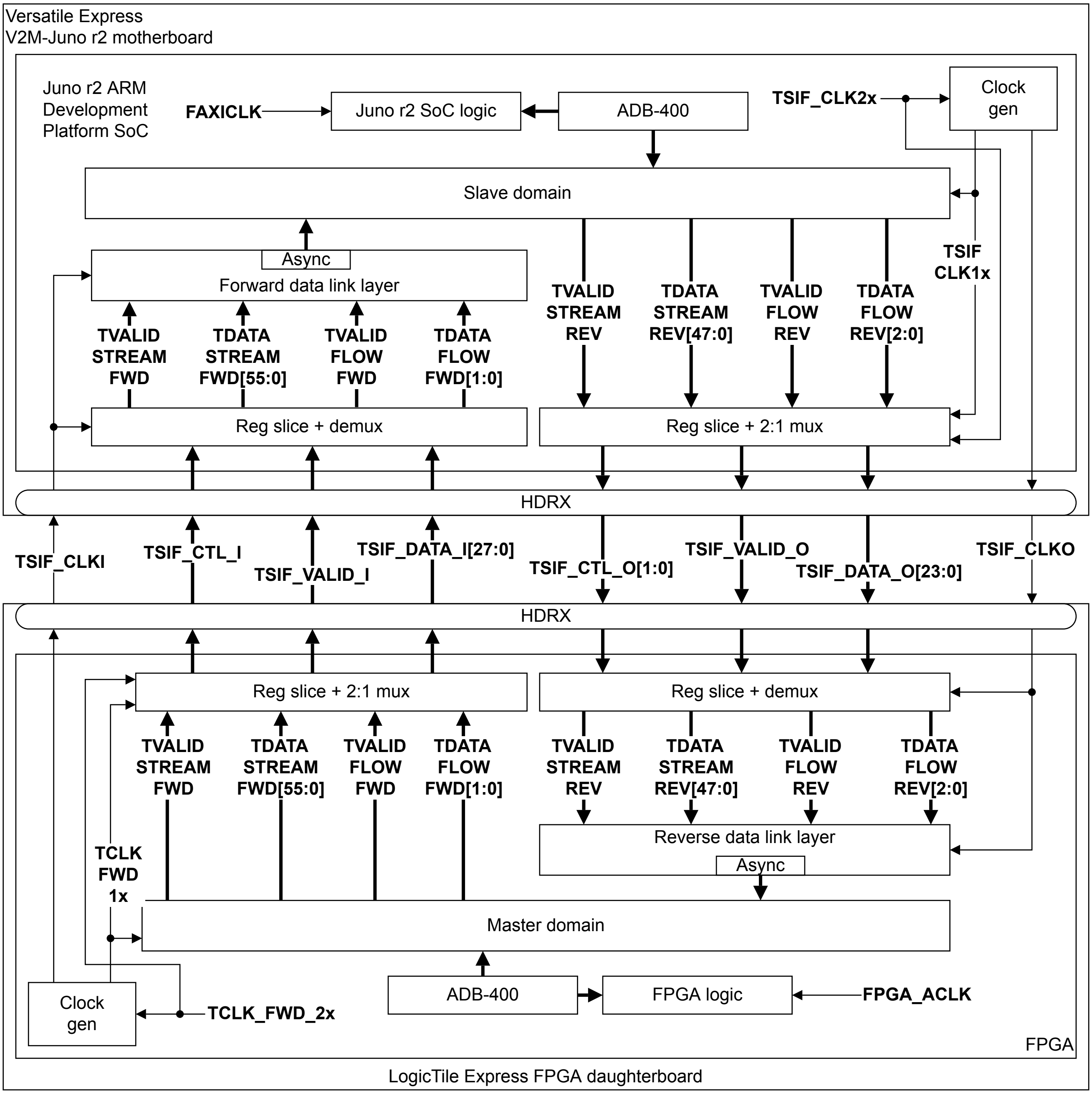


Figure 2-9 Thin Links non-coherent, AXI slave interface

Note

- Non-coherent mode is the default mode of the Thin Links slave interface.
- The Thin Links non-coherent AXI slave interface uses one fewer control bit than the ACE interface in each direction, and one more data bit than the ACE interface in each direction.

2.7.4 Thin Links slave interface in coherent mode

The following figure shows the Thin Links TLX-400 ACE slave interface on the Juno r2 SoC, that is, the slave interface in coherent mode, and its connection to the Thin Links TLX-400 master interface on the LogicTile daughterboard.

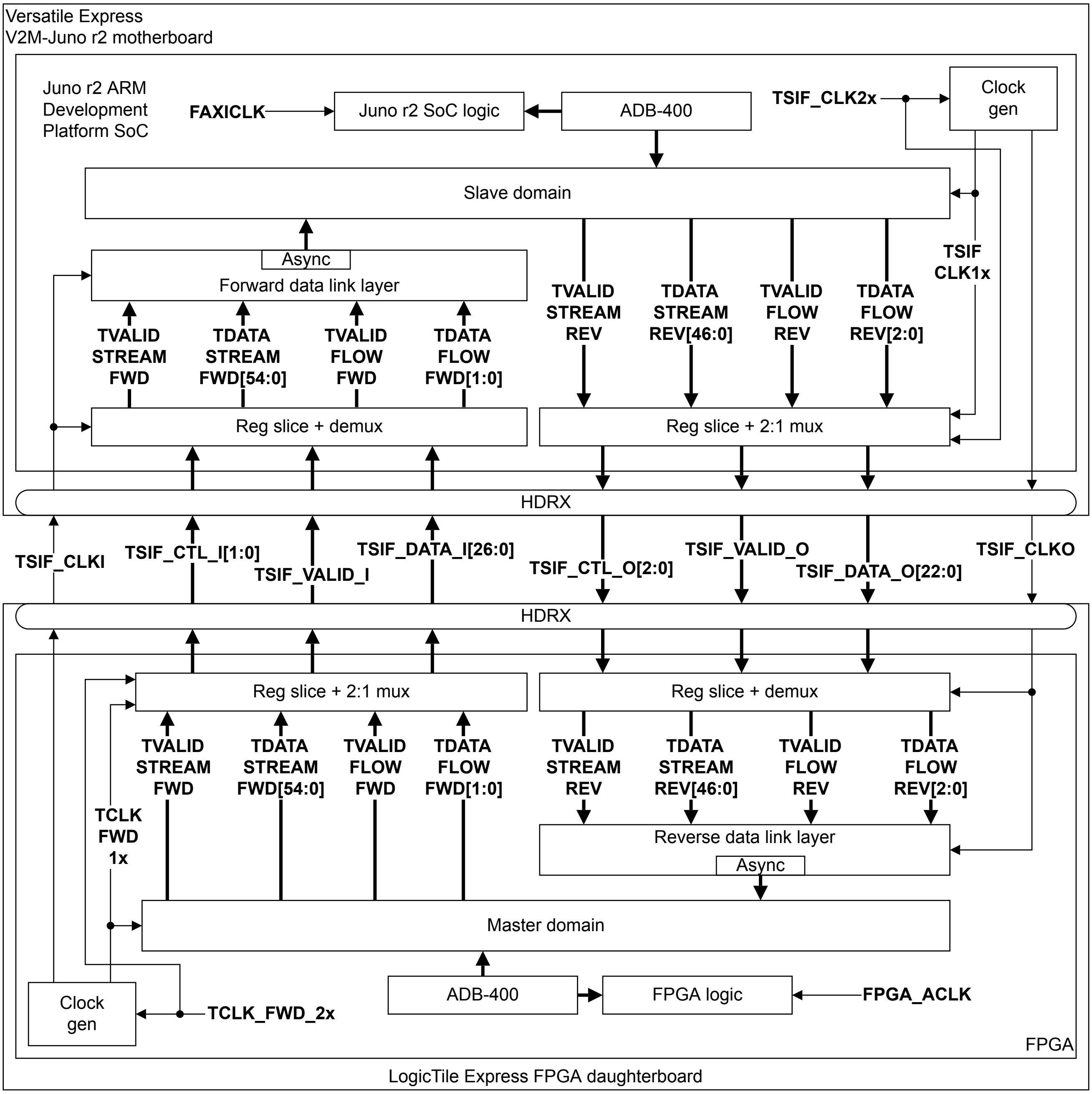


Figure 2-10 Thin Links ACE slave interface

Note

The Thin Links ACE slave interface uses one more control bit than the non-coherent, AXI interface in each direction, and one fewer data bit than the non-coherent, AXI interface in each direction.

2.8 IOFPGA

The IOFPGA provides access to low-bandwidth peripherals that the Juno r2 SoC does not provide. The Juno r2 SoC provides access to the IOFPGA through an SMC interface.

The following figure shows the internal architecture of the IOFPGA and its connectivity to external peripherals, including the external interrupts to the GIC-400 interrupt controller in the Juno r2 SoC.

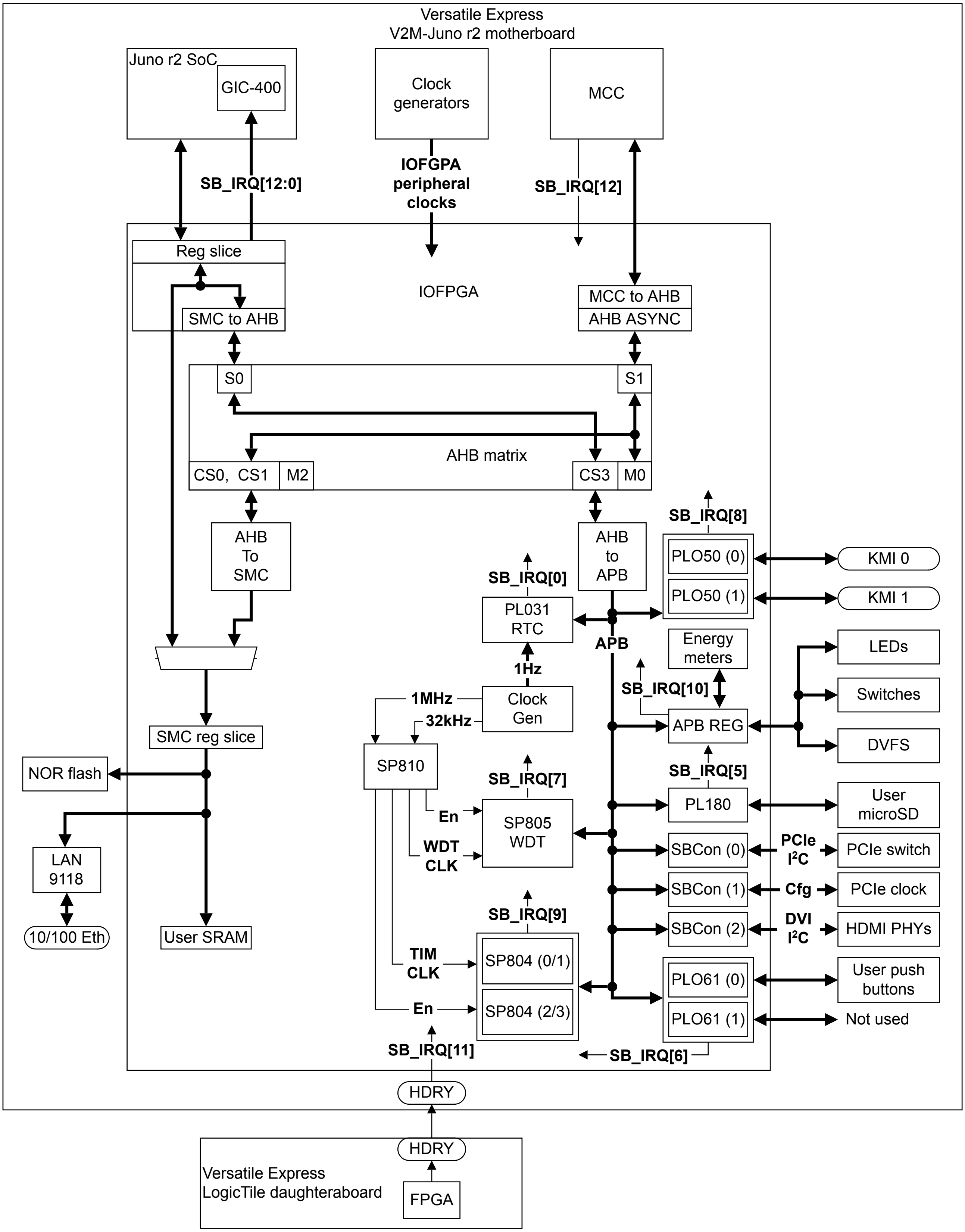


Figure 2-11 IOFPGA internal architecture

The following table shows the peripherals and buses inside the IOFPGA.

Peripheral	Interface or application	Release version
PL031	RTC.	r1p0.
PL050	Keyboard and mouse interfaces.	r1p0.
PL061	GPIO for additional user key entry and trusted keyboard entry.	r1p0.
PL180	User microSD card.	r1p0.
SP804	Dual-timer.	r2p0.
SP805	Watchdog Timer.	r2p0.
PL350 Series	SMC Controller.	r1p0.
AHB bus	-	AMBA 3 AHB-Lite Protocol Specification v1.0.
APB bus	-	AMBA 3 APB Protocol Specification v1.0.

Note

The peripheral versions apply to the Revision B V2M-Juno r2 motherboard.

Related concepts

4.2.2 IOFPGA system peripherals memory map on page 4-84.

2.9 HDLCD interface

Two HDMI PHYs on the V2M-Juno r2 motherboard provide video graphics.

Two HDLCD controllers in the Juno r2 SoC support all common 24-bit RGB formats. The HDLCD controllers are simple frame buffers whose RGB video connects to I/O drivers that drive the PHYs. The PHYs can operate at a maximum pixel clock frequency of 165MHz. This interface supports HDMI 1.4a up to 1080p.

A typical use of HDLCD0 is for lower resolution video than HDLCD1.

The HDLCD 24-bit data connects directly between Juno r2 SoC and the HDMI controllers on the V2M-Juno r2 motherboard. The HDMI controllers drive the HDMI connectors. The Juno r2 SoC configures the HDMI controllers at powerup or reset over the AP I^2C bus.

The HDMI controllers support I^2S audio from the Juno r2 SoC. They drive the audio to the HDMI connectors. The same audio stream connects to both HDMI connectors.

Note

Software that ARM supplies with the V2M-Juno r2 motherboard configures the Juno r2 SoC and board to enable correct operation of the HDLCD interface and correct HDMI output.

The following figure shows the HDLCD video system on the V2M-Juno r2 motherboard.

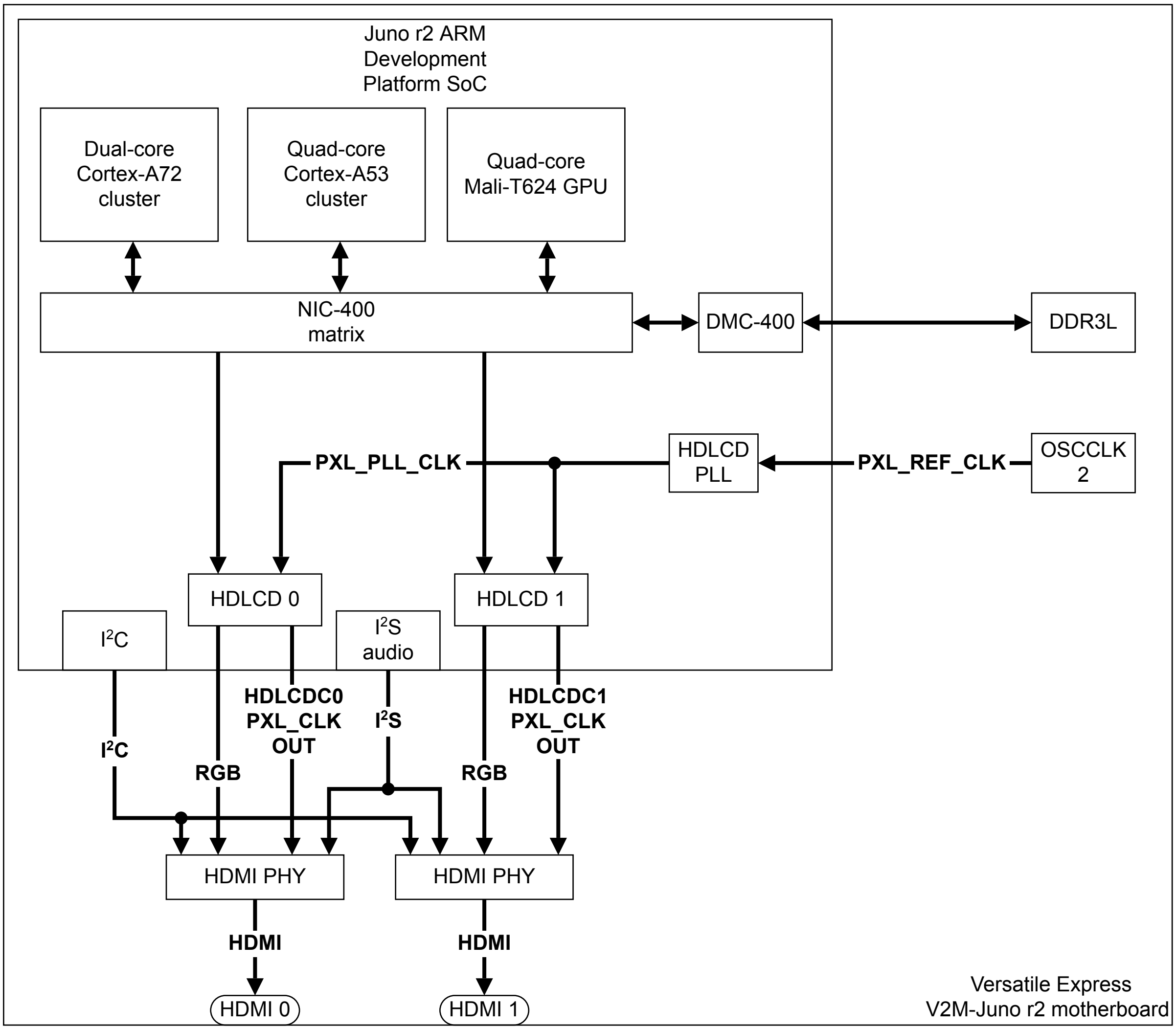


Figure 2-12 V2M-Juno r2 motherboard HDLCD interface

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.8 HDMI connectors on page Appx-A-131.

2.10 Interrupts

The Juno r2 SoC implements a GIC-400 Generic Interrupt Controller with the following external interrupts:

- Seven external interrupts connect to IOFPGA peripherals.
- One external interrupt connects to the SMC 10/100 Ethernet.
- One external interrupt connects to the MCC.
- One external interrupt connects to the LogicTile daughterboard site.
- The other three external interrupts are reserved.

The MCC generates its interrupt when you press the *ON/OFF/Soft Reset* push button. All interrupts connect to the GIC-400 in the Juno r2 SoC through the IOFPGA.

The following figure shows an overview of the external interrupt signals from the V2M-Juno r2 motherboard peripherals to the GIC-400 interrupt controller in the Juno r2 SoC.

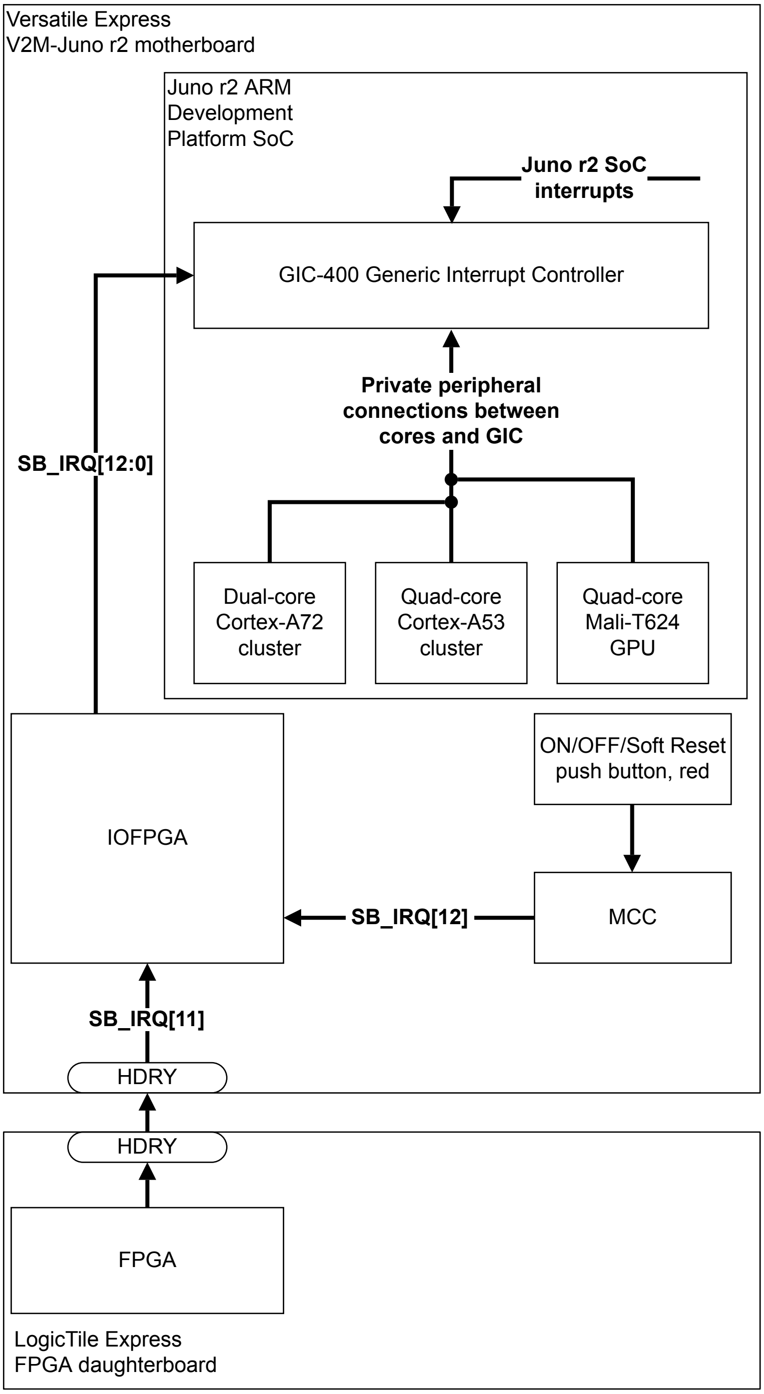


Figure 2-13 Juno r2 SoC interrupts overview

The following table shows the mapping of the external interrupt signals to the GIC-400 in the Juno r2 SoC. It lists the sources of the interrupts that originate in the V2M-Juno r2 motherboard or the LogicTile Express fitted in the daughterboard site.

Table 2-4 External interrupt signals to Juno r2 SoC

Interrupt ID	GIC IRQ ID	Motherboard signal name	Source
96-99	64-67	-	Juno r2 SoC internal peripherals and systems.
100	68	**SB_IRQ[0]**	IOFPGA-PL031 RTC.

Table 2-4 External interrupt signals to Juno r2 SoC (continued)

Interrupt ID	GIC IRQ ID	Motherboard signal name	Source
101-102	69-70	**SB_IRQ[2:1]**	IOFPGA-Reserved interrupts.
103-191	71-159	-	Juno r2 SoC internal peripherals and systems.
192	160	**SB_IRQ[3]**	IOFPGA-SMC 10/100 Ethernet.
193	161	**SB_IRQ[4]**	IOFPGA-Reserved interrupt.
194	162	**SB_IRQ[5]**	IOFPGA-PL180 user microsSD card.
195	163	**SB_IRQ[6]**	IOFPGA-PL061 GPIO (0) and GPIO (1) used for additional user key entry.
196	164	**SB_IRQ[7]**	IOFPGA-SP805 WDT.
197	165	**SB_IRQ[8]**	IOFPGA-PL050 Keyboard and mouse interface.
198	166	**SB_IRQ[9]**	IOFPGA-SP804 Dual-timer (0-1) and SP804 dual-timer (2-3).
199	167	**SB_IRQ[10]**	IOFPGA:APB system registers from SYS_MISC[SWINT] Register.
200	168	**SB_IRQ[11]**	LogicTile FPGA daughterboard. Interrupt from FPGA on LogicTile daughterboard.
201	169	**SB_IRQ[12]**	MCC-Interrupt generated by pressing the *ON/OFF/Soft Reset* push button.
202-223	170-191	-	Juno r2 SoC internal peripherals and systems.

See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* for information on the interrupts from the systems in the Juno r2 SoC.

2.11 USB 2.0 interface

The Juno r2 SoC provides a USB 2.0 interface. The interface is capable of 480Mbps.

The host controller on the Juno r2 SoC connects to an external PHY on the V2M-Juno r2 motherboard. This PHY connects to a four-port hub that connects to four USB 2.0 user ports.

Each port can supply 1A to an external load.

The following figure shows the USB 2.0 system, the host controller, PHY, and hub.

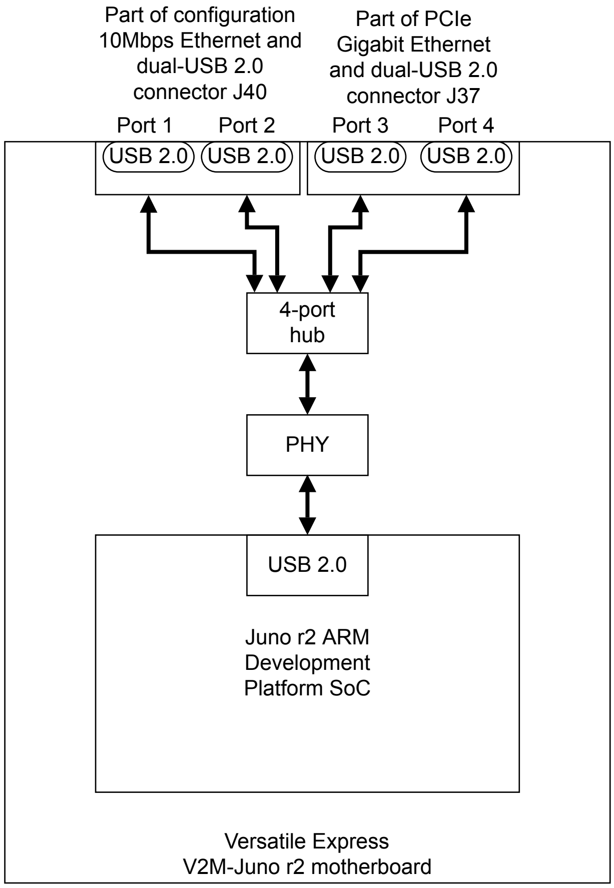


Figure 2-14 V2M-Juno r2 motherboard USB 2.0 interface

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.2 Configuration 10Mbps Ethernet and dual-USB connector on page Appx-A-125.

A.3 PCI Express Gigabit Ethernet and dual-USB connector on page Appx-A-126.

2.12 SMC 10/100 Ethernet interface

The Juno r2 SoC provides a 10/100 Ethernet port.

This port connects to the *Static Memory Controller* (SMC) bus through a LAN9118 Ethernet controller and the IOFPGA. The LAN9118 Ethernet controller is mapped to chip select CS2 of the PL354 SMC memory controller at base address `0x18000000`. See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)*.

The following figure shows the SMC 10/100 Ethernet interface.

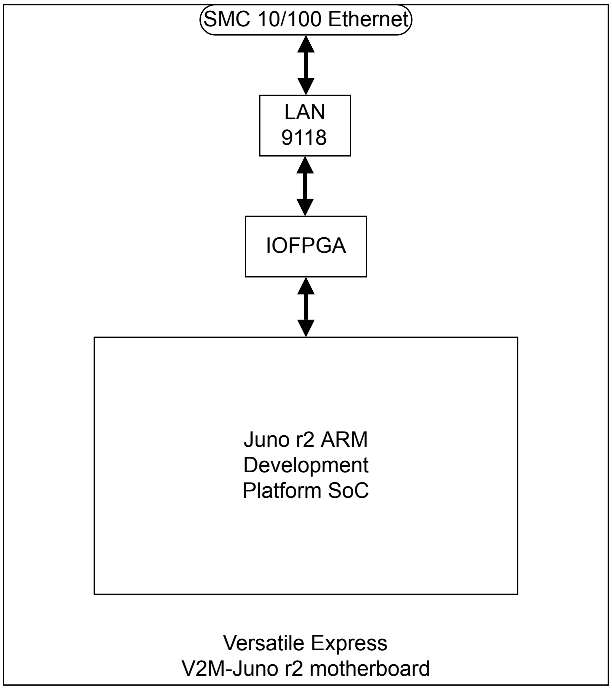


Figure 2-15 V2M-Juno r2 motherboard SMC 10/100 Ethernet interface

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.4 SMC 10/100 Ethernet connector on page Appx-A-127.

2.13 UART interface

The Juno r2 SoC provides a dual-port UART interface.

The UART 0 transceiver can connect to one of the following:

- The MCC.
- The UART 0 interface on the Juno r2 SoC.

The UART 1 transceiver can connect to one of the following:

- The Daughterboard Configuration Controller on the LogicTile daughterboard.
- The UART 1 interface on the Juno r2 SoC.
- The MCC.

Variables *`MBLOG`* and *`DBLOG`* in the `config.txt` file define the connections of the UART transceivers.

The *`MBLOG`* options are:

`FALSE`	MCC not connected. The Juno r2 SoC UART 0 interface connects to the UART 0 transceiver.
`UART0`	The MCC connects to the UART 0 transceiver.
`UART1`	The MCC connects to the UART 1 transceiver.

The *`DBLOG`* options are:

`FALSE`	Daughterboard Configuration Controller not connected. The Juno r2 SoC UART 1 interface connects to the UART 1 transceiver.
`UART1`	The Daughterboard Configuration Controller connects to the UART 1 transceiver.

Note

If you set option `UART1` for both *`MBLOG`* and *`DBLOG`*, *`MBLOG`* overrides *`DBLOG`* and the UART 1 transceiver connects to the MCC, UART 0 transceiver connects to the UART 0 interface on the Juno r2 SoC, and the Daughterboard Configuration Controller is not connected.

The default connection of the UART 0 transceiver is to the MCC at powerup and then it switches to the Juno r2 SoC UART 0 interface.

The default connection of the UART 1 transceiver is to the Daughterboard Configuration Controller at powerup and then it switches to the Juno r2 SoC UART 1 interface.

The following figure shows the UART interface to the V2M-Juno r2 motherboard.

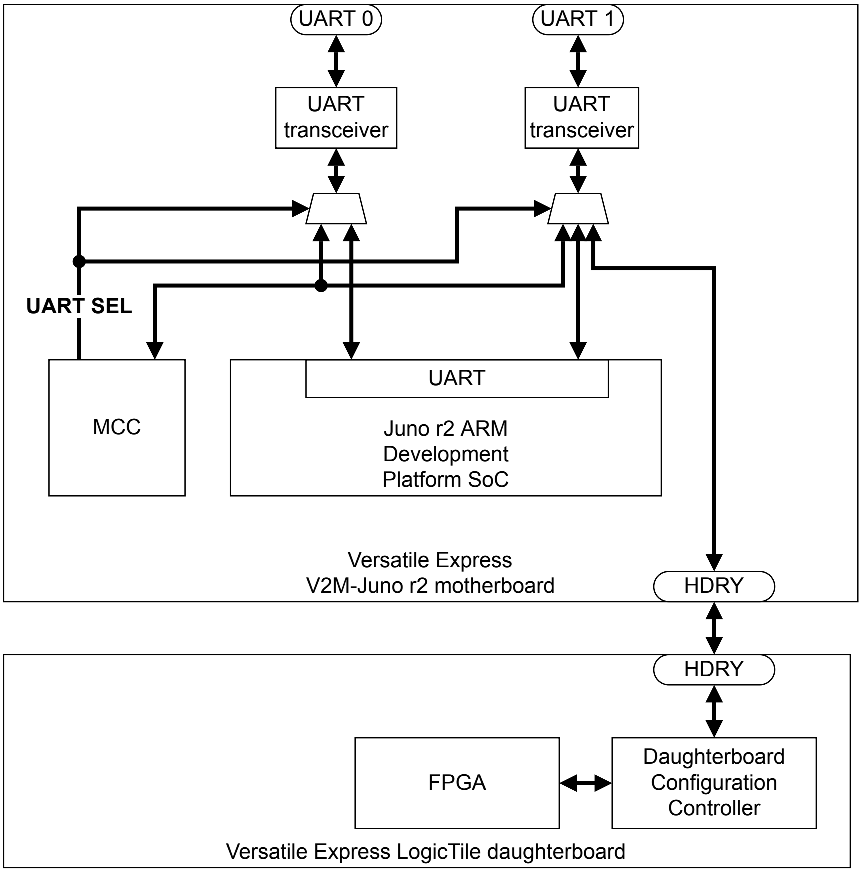


Figure 2-16 V2M-Juno r2 motherboard UART interface

Related concepts

2.13 UART interface on page 2-52.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.11 Dual-UART connector on page Appx-A-142.

2.14 PCI Express system

The Juno r2 SoC provides a PCIe Gen 2 4-lane root complex and PHY that connects to a PCIe Gen 2 switch on the V2M-Juno r2 motherboard.

This section contains the following subsections:

- *2.14.1 Overview of PCI Express system* on page 2-54.
- *2.14.2 PCI Express expansion slots* on page 2-54.
- *2.14.3 SATA 2.0 ports* on page 2-55.
- *2.14.4 Gigabit Ethernet port* on page 2-55.

2.14.1 Overview of PCI Express system

The V2M-Juno r2 motherboard provides a PCIe switch that provides access through four PCIe slots, two SATA 2.0 ports, and one Gigabit Ethernet port. The Juno r2 SoC implements a PCIe Gen 2 root complex and PHY.

The following figure shows the V2M-Juno r2 motherboard PCIe system.

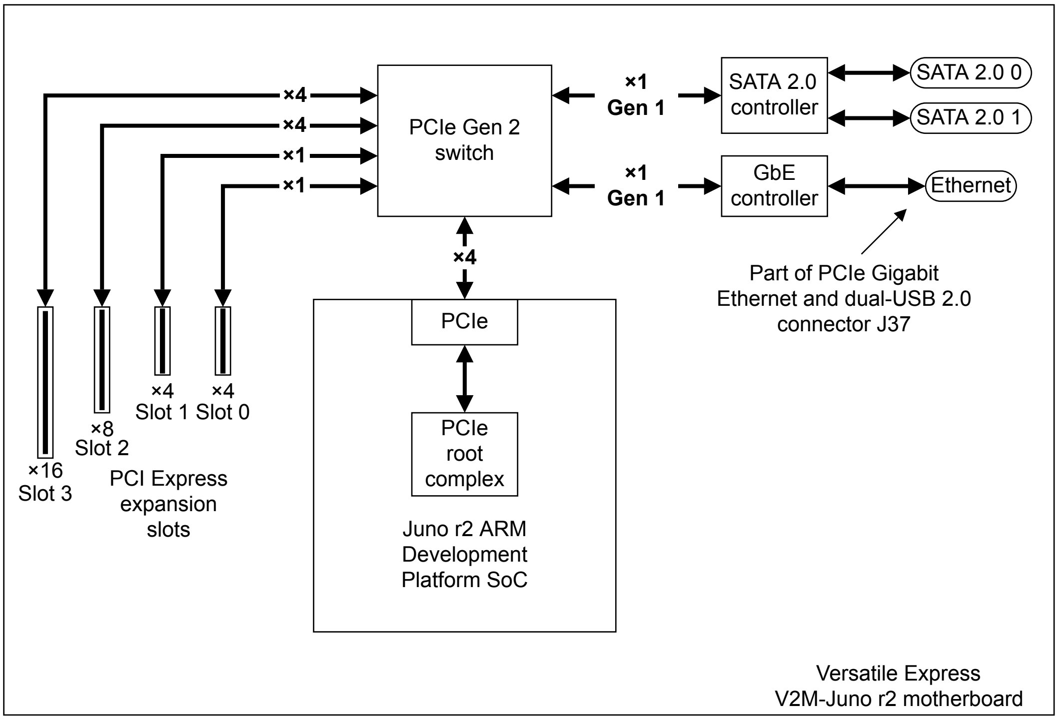


Figure 2-17 V2M-Juno r2 motherboard PCIe system

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

2.14.2 PCI Express expansion slots

The PCIe Gen 2 switch connects to four PCIe expansion slots on the V2M-Juno r2 motherboard.

The following table shows the four PCIe expansion slots on the V2M-Juno r2 motherboard.

Table 2-5 PCI Express expansion slots

Slot number	Connector size-PCIe lanes	Used lanes	Unused lanes
Slot 0	×4	1	3
Slot 1	×4	1	3

Table 2-5 PCI Express expansion slots (continued)

Slot number	Connector size-PCIe lanes	Used lanes	Unused lanes
Slot 2	×8	4	4
Slot 3	×16	4	12

Related references

A.9.1 PCI Express ×4 connectors, one-lane slot 0 and slot 1 on page Appx-A-132.

A.9.2 PCI Express ×8 connector, four-lane slot 2 on page Appx-A-134.

A.9.3 PCI Express ×16 connector, four-lane slot 3 on page Appx-A-136.

2.14.3 SATA 2.0 ports

The PCIe switch connects to the SATA 2.0 controller through a single-lane PCIe port.

The SATA 2.0 controller drives two SATA 2.0 ports for hard drives:
- The SATA 2.0 controller is a Silicon Image Sil3232 SATA 2.0 controller with a x1 Gen 1 connection to the PCIe switch.
- The connections between the SATA 2.0 ports and the SATA 2.0 controller have a Serial ATA Generation 2 transfer rate of 3.0 Gbps, 300MBs.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.10 SATA 2.0 connectors on page Appx-A-140.

2.14.4 Gigabit Ethernet port

The PCIe switch connects to the Gigabit Ethernet controller over a single-lane PCIe Gen 1 connection.

The controller is a Marvell 88E8057-A0-NNB2C000 Gigabit Ethernet controller.

The Gigabit Ethernet controller drives a single Gigabit Ethernet port on the V2M-Juno r2 motherboard.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.3 PCI Express Gigabit Ethernet and dual-USB connector on page Appx-A-126.

2.15 Keyboard and mouse interface

The V2M-Juno r2 motherboard provides two KMI ports for PS/2 keyboard and mouse input to the system.

The keyboard and mouse inputs connect to PL050 interfaces in the IOFPGA.

The following figure shows the V2M-Juno r2 motherboard KMI interface.

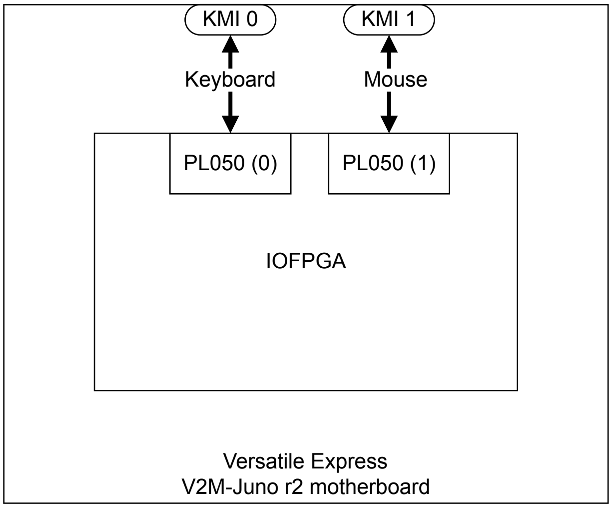


Figure 2-18 V2M-Juno r2 motherboard KMI interface

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.7 Keyboard and Mouse Interface (KMI) connector on page Appx-A-130.

2.16 Additional user key entry

The V2M-Juno r2 motherboard provides the following methods of additional user key entry:

- Trusted keyboard entry using the secure keyboard entry port on the Juno r2 SoC:
  - This method requires a custom external device with decode circuitry for key entry.
  - The Juno r2 SoC controls the trusted keyboard over a secure I^2C bus.
  - Supports touch screen display. A touch screen secure keyboard interface board with a built-in controller enables use of a resistive touch screen.
- Six user push buttons on the V2M-Juno r2 motherboard that emulate hand-held devices. The push buttons provide access through IOFPGA GPIO.

A single 9-pin Mini-Din socket on the top face of the V2M-Juno r2 motherboard provides a secure keyboard entry port for text entry using an external keyboard. The following figure shows the additional user key interface and its connections to the user push buttons on the V2M-Juno r2 motherboard.

Note

One user push button input, *NU/NMI*, to the FPGA is not available to the external secure keyboard custom device.

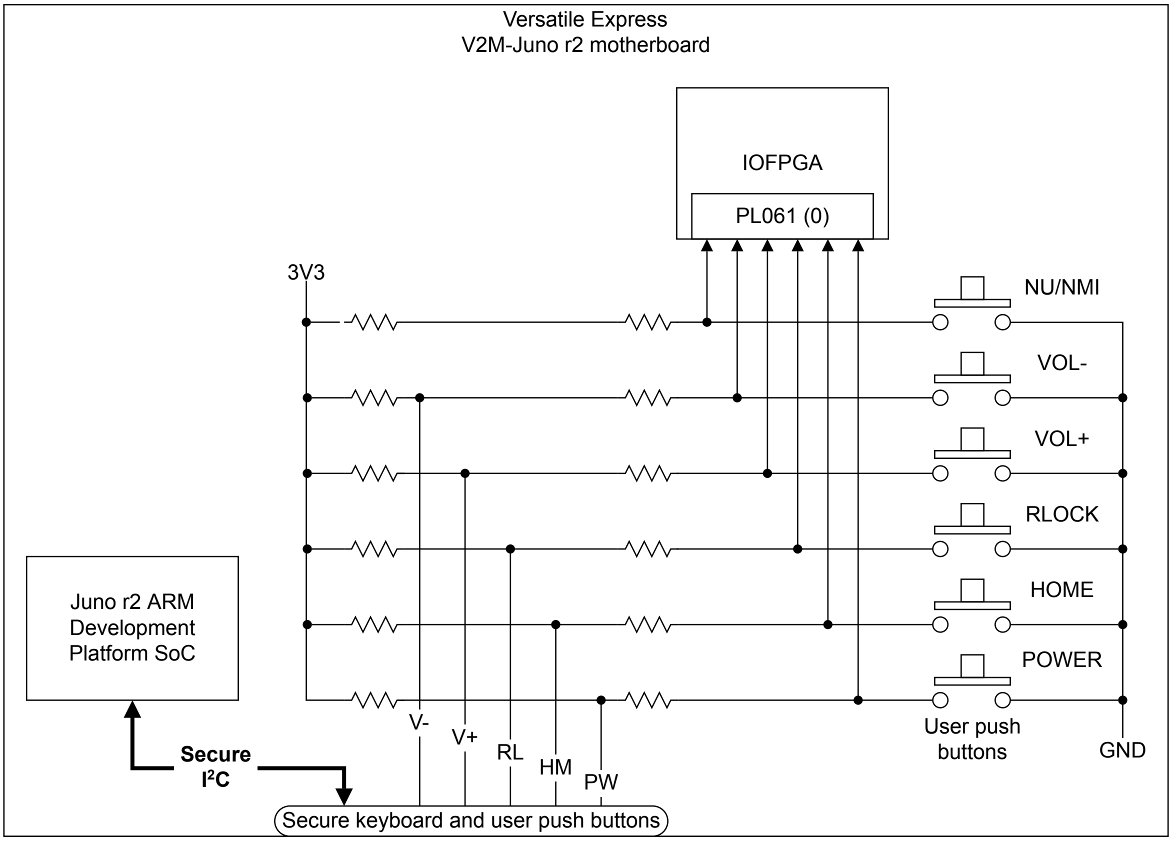


Figure 2-19 Additional user key entry interface

The following figure shows an example trusted keyboard design using an external custom device that connects to the secure keyboard entry port.

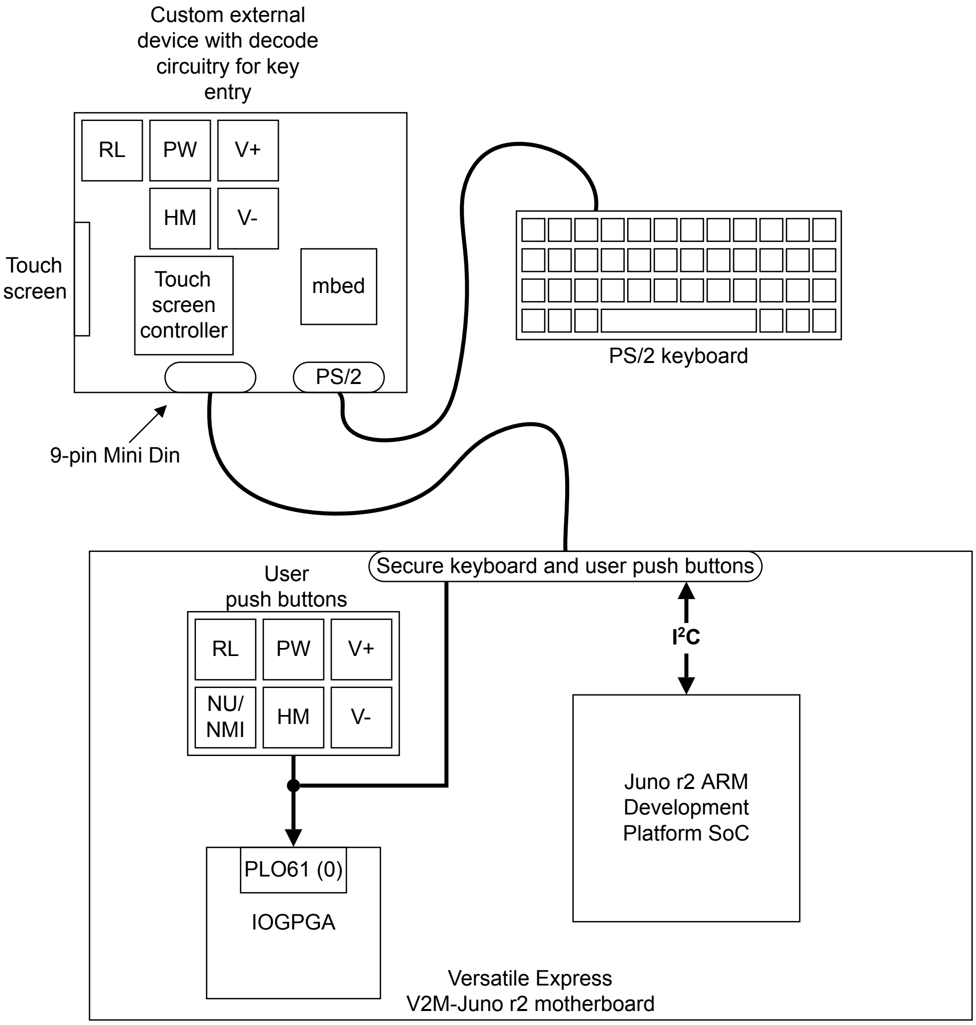


Figure 2-20 Example trusted keyboard design

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.
1.4 Connectors on front and rear panels on page 1-16.
A.12 Secure keyboard and user push buttons connector on page Appx-A-144.

2.17 Debug and trace

The V2M-Juno r2 motherboard supports processor debug, P-JTAG, 16-bit and 32-bit trace to enable sofware debug and trace in the Juno r2 SoC.

You connect a debug unit to the P-JTAG connector on the V2M-Juno r2 motherboard to run processor debug, P-JTAG.

Note

The processor debug device can be any compatible debug unit, for example DSTREAM, or a compatible third-party debugger.

You connect a compatible trace port analyzer, for example DSTREAM, or a compatible third-party debugger, to the *TRACEA-SINGLE* connector to run 16-bit trace or to both the *TRACEA-SINGLE* and *TRACEB-DUAL* connector to run 32-bit trace.

The following figure shows an overview of the V2M-Juno r2 motherboard debug and trace architecture.

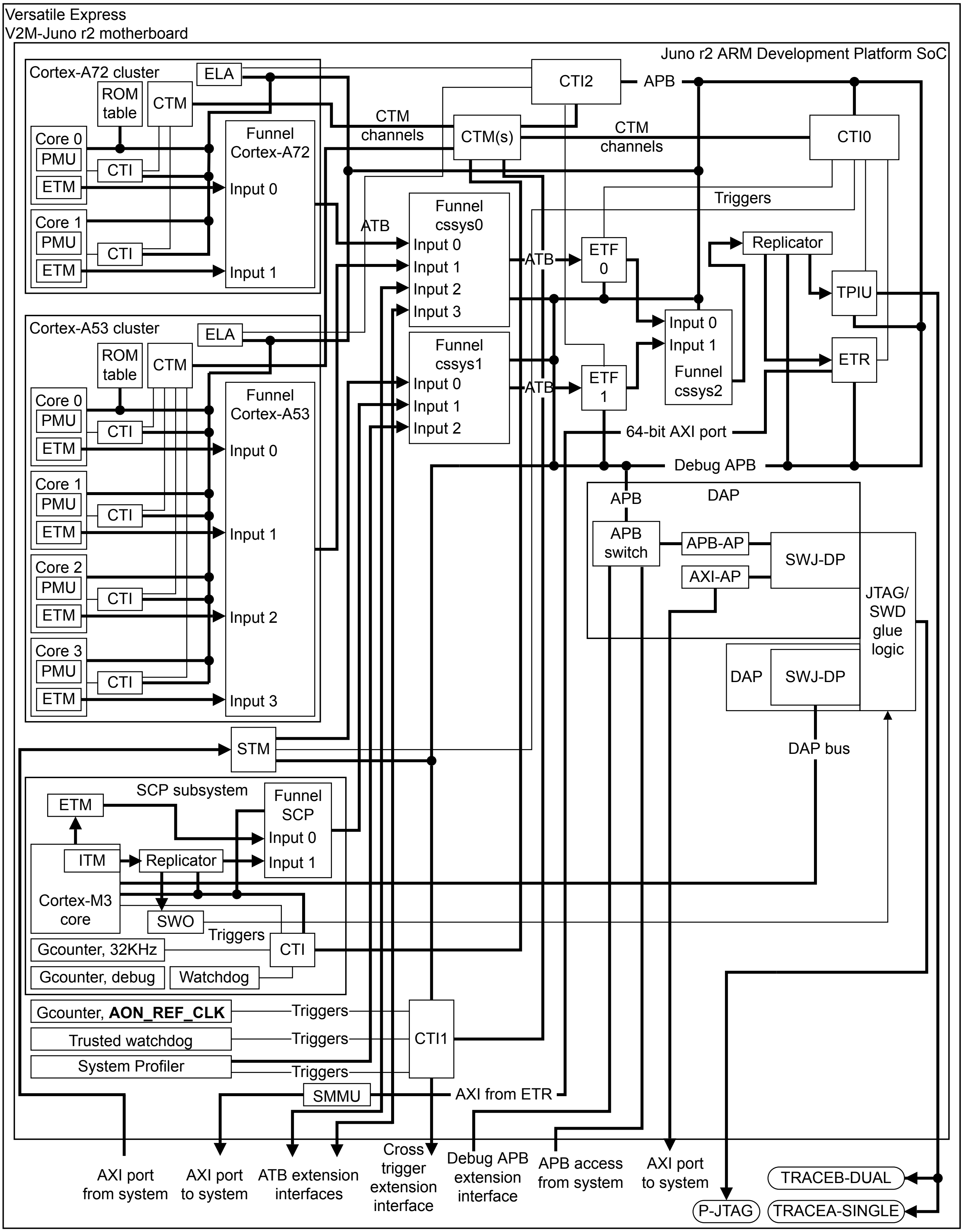


Figure 2-21 V2M-Juno r2 motherboard debug architecture

See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* for more information on the Juno r2 SoC debug architecture.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.1.1 P-JTAG connector on page Appx-A-121.

A.1.2 Trace connectors on page Appx-A-122.

Chapter 3

Configuration

This chapter describes the powerup and configuration process of the Versatile Express V2M-Juno r2 motherboard.

It contains the following sections:

3.1 Overview of the V2M-Juno r2 motherboard configuration system

The V2M-Juno r2 motherboard provides hardware infrastructure to enable board configuration during powerup or reset. The MCC, in association with the configuration microSD card, configures the V2M-Juno r2 motherboard during powerup or reset.

When the configuration process starts after application of power, or pressing the *ON/OFF/Soft Reset* button, the configuration process completes without further intervention from the user.

The MCC controls the transitions of the V2M-Juno r2 motherboard between the operating states in response to pressing the reset buttons or powerdown requests from the operating system.

The following figure shows the V2M-Juno r2 motherboard configuration system.

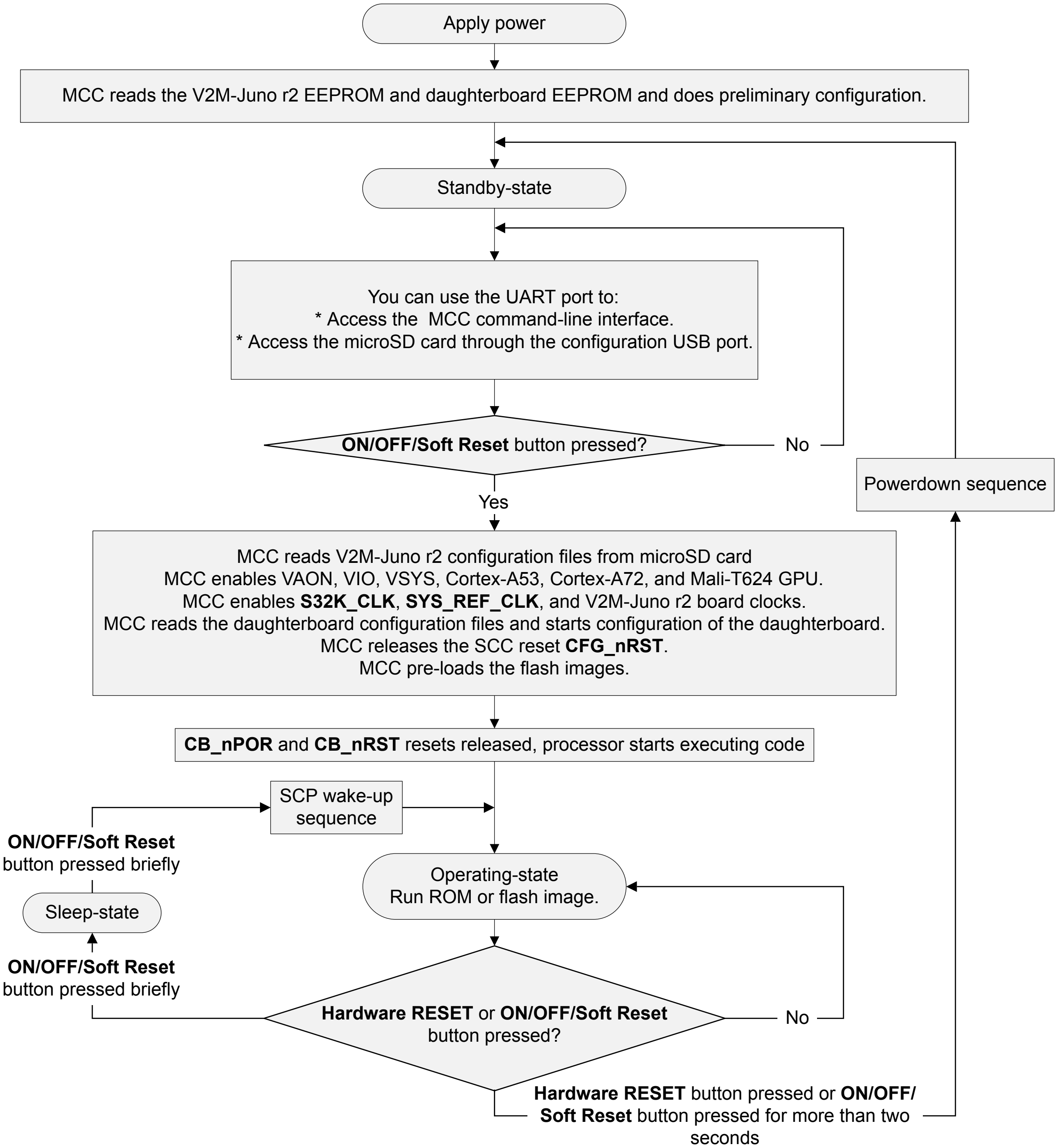


Figure 3-1 V2M-Juno r2 motherboard configuration system

The configuration microSD card stores the V2M-Juno r2 motherboard configuration files, including the `board.txt` file. You can access the microSD card as a *Universal Serial Bus Mass Storage Device* (USBMSD).

The EEPROM contains the following information that the MCC uses during the configuration process:

- Board HBI number.
- Board revision.
- Board variant.
- Number of FPGAs.
- Names of the current images in 8.3 format and the file creation dates.
- Juno r2 SoC calibration data.

Note

- The HBI number is a unique code that identifies the board. The root directories of the microSD card contain sub-directories in the form *HBI<BoardNumber><Boardrevision>*, for example HBI0262D. HBI0262D is the HBI number of the V2M-Juno r2 motherboard.
- If the MCC does not find a configuration directory that matches the HBI number of the board, the configuration process fails and the board enters the standby-state.

3.2 Configuration process and operating modes

The V2M-Juno r2 motherboard provides a powerup and configuration process, a powerdown process, and two operating modes, operating-state and sleep-state.

This section contains the following subsections:

- *3.2.1 Transitions between operating modes* on page 3-65.
- *3.2.2 Powerup and configuration sequence* on page 3-66.
- *3.2.3 Powerdown sequence* on page 3-67.
- *3.2.4 Sleep-state sequence* on page 3-68.
- *3.2.5 Wake-up sequence* on page 3-68.

3.2.1 Transitions between operating modes

The power reset push buttons and configuration files control the sequence of events of the powerup and configuration process and the transitions between the different states of the V2M-Juno r2 motherboard.

The V2M-Juno r2 motherboard has the following operating modes:

Standby-state

The V2M-Juno r2 motherboard and Juno r2 SoC are mostly powered down. The powerup and configuration sequence takes them to the operating-state.

Operating-state

This is the full operating mode. Peripherals, clocks, and application code all operate. The powerdown sequence takes the board to the standby-state and the sleep-state sequence takes it to the sleep-state.

Sleep-state

This state powers down the Juno r2 SoC clusters and preserves operating data and the application code start-point. Application code resumes when the Juno r2 SoC returns to the operating-state.

Note

The system cannot return directly to the standby-state from the sleep-state. It must return to the operating-state before the powerdown sequence can begin.

The following figure shows the configuration process and the transitions between the standby-state, operating-state, and sleep-state of the V2M-Juno r2 motherboard.

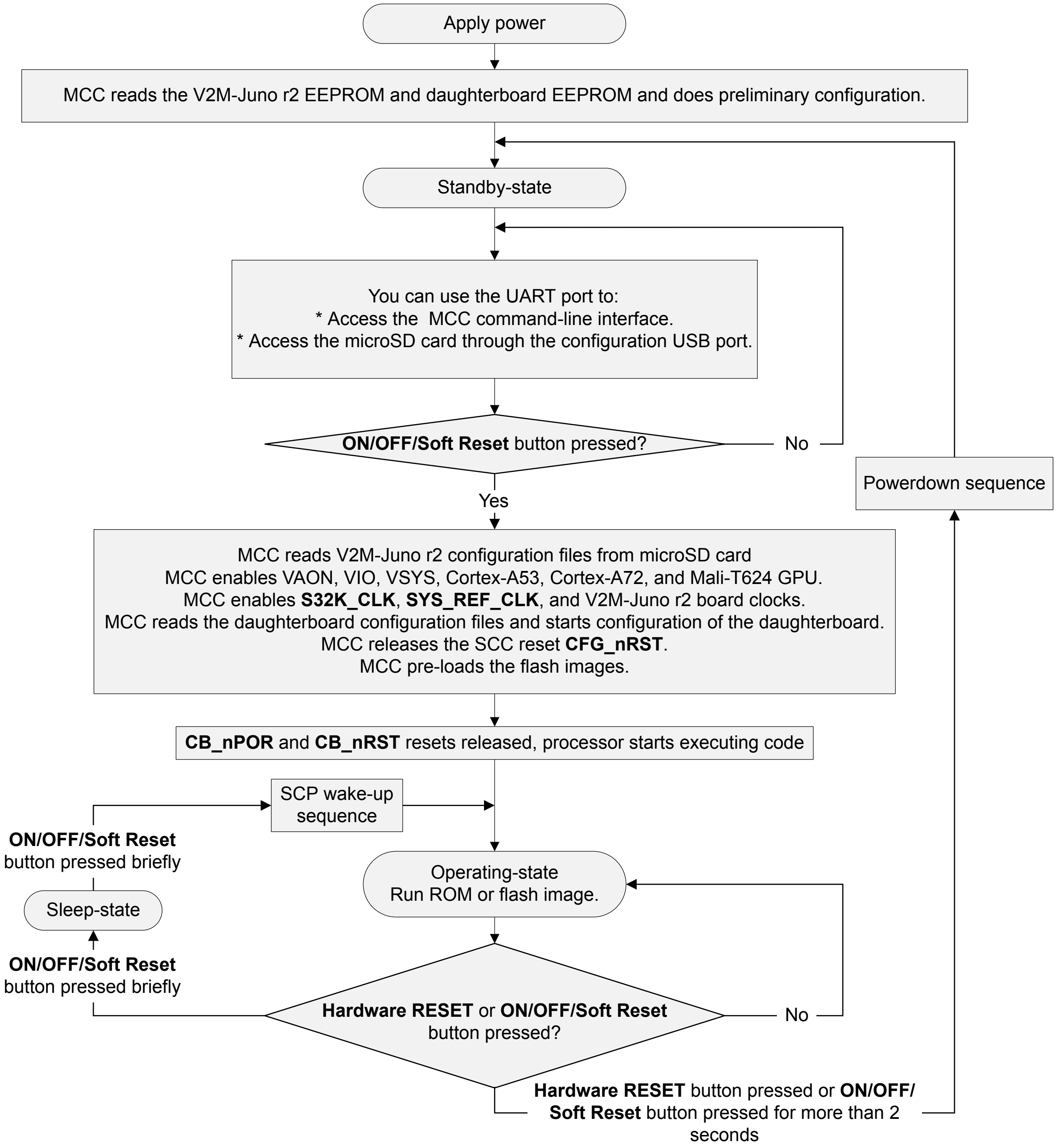


Figure 3-2 Transitions between standby-state, operating-state, and sleep-state

3.2.2 Powerup and configuration sequence

The powerup and configuration sequence takes the V2M-Juno r2 motherboard from the standby-state to the operating-state.

Pressing the *On/Off Soft Reset* button initiates the following sequence:

1. The board applies power to the system.
2. The MCC powers the EEPROM on the V2M-Juno r2 motherboard and the EEPROM on any fitted LogicTile daughterboard and reads them to determine the HBI identification codes for the boards.
3. The system enters the standby-state.
4. The system enables the MCC command-line interface on the UART.

5. The system enables the configuration microSD memory card and you can connect a workstation to the configuration USB port or configuration Ethernet port to edit existing configuration files or *Drag-and-Drop* new configuration files.
6. The system remains in standby-state until you press the *ON/OFF/Soft Reset* push button or you send the `REBOOT` command to the MCC command-line interface.
7. The system loads the board configuration file:
   - The MCC reads the generic `config.txt` file.
   - The MCC searches the configuration microSD card `MB` directory for the V2M-Juno r2 motherboard HBI0262D subdirectory that matches the HBI code in the EEPROM.
   - If a LogicTile daughterboard is fitted, the MCC searches the configuration microSD card `SITE2` directory for a subdirectory that matches the HBI code in the fitted LogicTile EEPROM.
8. The next steps depend on the configuration files:
   - If the MCC finds configuration subdirectories that match the HBI code of the V2M-Juno r2 motherboard and any fitted LogicTile daughterboard, configuration continues and the MCC reads the daughterboard `board.txt` file.
   - If the MCC does not find the correct configuration files, it records the failure to a log file on the configuration microSD card. Configuration stops and the system reenters standby-state.
9. The MCC switches on the ATX PSU and power domains in the Juno r2 SoC using the board power controller PMIC.
10. The MCC enables the SCP 32kHz clock, **SYS_REF_CLK** on the Juno r2 SoC, and clock generators on the V2M-Juno r2 motherboard.
    - The SCP in the Juno r2 SoC boots from internal ROM and then performs the basic setup of the Juno r2 SoC including the PLLs, internal clocks, and peripherals inside the Juno r2 SoC.
    - The SCP releases the *Power Policy Units* (PPUs) to start the cluster boot sequences.
11. The MCC measures the board power supplies.
12. The MCC reads the IOFPGA image from the configuration microSD card and loads it into the IOFPGA.
13. The MCC sets the board oscillator frequencies using values from the `board.txt` file.
14. If the MCC finds new software images, it loads them into the flash through the IOPGA.
15. The MCC releases the SCC reset **CFG_nRST**.
16. The MCC configures the Juno r2 SoC SCC registers using values from the `board.txt` file.
17. The MCC releases the system resets **CB_nPOR** and **CB_nRST** and the system enters the operating-state.

    ——— **Note** ———

    The **CB_nPOR** signal drives the **nPORESET** signal inside the Juno r2 SoC.

    ———————————

18. The application code runs. Normal operation continues until a reset occurs:
    - Any of the following actions initiates the powerdown sequence and puts the V2M-Juno r2 motherboard into the standby-state:
      — Pressing the *Hardware Reset* button.
      — Pressing and holding the *On/Off/Soft Reset* button for more than two seconds.
      — A powerdown request from the operating system.
    - A short press of the *On/Off/Soft Reset* button, less than two seconds, initiates the sleep-state sequence and puts the V2M-Juno r2 motherboard into the sleep-state.

3.2.3 Powerdown sequence

The powerdown sequence takes the V2M-Juno r2 motherboard from the operating-state to the standby-state.

The powerdown sequence is as follows:

1. The powerdown sequence begins with one of the following:

  - Pressing the *Hardware Reset* button.
  - Pressing and holding the *On/Off Soft Reset* button for more than two seconds.
  - A powerdown request from the operating system.
2. The *System Control Processor* (SCP) signals a powerdown request to the application cluster, that is, either the Cortex-A72 cluster or the Cortex-A53 cluster.
3. The application cluster goes through its cleanup and shutdown sequence.
4. The application cluster goes to the *Wait for Interrupt* (WFI) state.
5. The *Power Policy Unit* (PPU) sees the WFI state and powers down.

   Note

   The SCP waits for this sequence to complete.

6. The SCP powers down the Cortex-A53, Cortex-A72, VSYS, and Mali-T624 GPU.
7. The SCP signals to the MCC, using the *Power Management IC* (PMIC), *Ready for Shutdown*.
8. The MCC applies **CB_nPOR** and disables the board clocks and the PMIC.

   Note

   The **CB_nPOR** signal drives the **nPORESET** signal inside the Juno r2 SoC.

9. The V2M-Juno r2 motherboard is in the standby-state until pressing the *On/Off/Soft Reset* button initiates the powerup and configuration sequence.

3.2.4 Sleep-state sequence

The sleep-state is a low power mode of the Juno r2 SoC that preserves operating data and the application code state. The sleep-mode sequence takes the Juno r2 SoC from the operating-state to the sleep-state.

The operating-state to sleep-state sequence is as follows:

1. A short press of the *On/Off/Soft Reset* button, less than two seconds.

   Warning

   Pressing and holding the *On/Off/Soft Reset* button for more than two seconds initiates the powerdown sequence and puts the V2M-Juno r2 motherboard into the standby-state. This might result in loss of data.

2. The *System Control Processor* (SCP) sends the *Message Handling Unit* (MHU) sleep command to the application cluster, that is, either the Cortex-A72 or Cortex-A53.
3. The application cluster goes through its cleanup and shutdown sequence. The application cluster goes to the *Wait for Interrupt* (WFI) state.
4. The *Power Policy Unit* (PPU) sees the WFI state and powers down.

   Note

   The SCP waits for this sequence to complete.

5. The SCP powers down the Cortex-A53, Cortex-A72, VSYS, and Mali-T624 GPU.
6. The SCP maintains on-chip RAM and secure RAM data. This data is available when the Juno r2 SoC returns to the operating-state.
7. The Juno r2 SoC is in the sleep-state until a short press, less than two seconds, of the *On/Off/Soft Reset* button initiates the wake up sequence and returns it to the operating-state.

3.2.5 Wake-up sequence

The wake-up sequence takes the Juno r2 SoC from the sleep-state to the operating-state. Application software resumes operation from the previous operating point with all data restored.

The sleep-state to operating-state sequence is as follows:

1. A short press of the *On/Off/Soft Reset* button, less than two seconds.
2. The *System Control Processor* (SCP) enables the Cortex-A72, Cortex-A53, VSYS, and the Mali-T624 GPU.
3. The SCP performs basic Juno r2 SoC setup, PLLs, internal clocks, and test chip peripherals.
4. The SCP writes state data to on-chip secure RAM so that the application cluster, that is, either the Cortex-A72 or Cortex-A53, resumes in the correct state and does not boot up from standby.
5. The SCP releases the *Power Policy Unit* (PPU) to start the application cluster boot sequence.
6. The application code resumes from the point when the Juno r2 SoC went into the sleep-state.

3.3 Configuration files

Configuration files in the configuration microSD card control the board powerup and configuration process.

This section contains the following subsections:

- *3.3.1 Overview of configuration files and microSD card directory structure* on page 3-70.
- *3.3.2 `config.txt` generic motherboard configuration file* on page 3-72.
- *3.3.3 Contents of the `MB` directory* on page 3-72.
- *3.3.4 Contents of the `SITE1` directory* on page 3-73.
- *3.3.5 Contents of the `SITE2` directory* on page 3-74.
- *3.3.6 Contents of the `SOFTWARE` directory* on page 3-74.

3.3.1 Overview of configuration files and microSD card directory structure

Because the V2M-Juno r2 motherboard configuration microSD card is non-volatile flash memory, it is only necessary to load new configuration files if you change the system configuration. The configuration microSD card contains default configuration files.

If you connect a workstation to the configuration USB port or configuration Ethernet port, the configuration memory device, that is, the configuration microSD card, appears as a *USB Mass Storage Device* (USBMSD) and you can add, edit, or delete files.

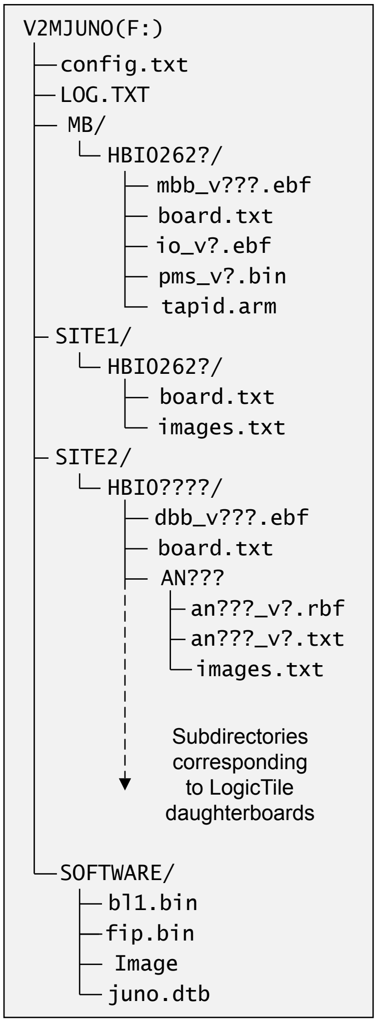
You can use a standard text editor that produces DOS line endings to read and edit the board configuration files.

The following figure shows a typical example of the directory structure in the microSD card memory.

Caution

Files names and directory names are in 8.3 format:

- File names that you generate must be in lower case.
- Directory names must be in upper case.
- All configuration files must end in DOS line endings, `0x0D`/`0x0A`.



```
V2MJUNO(F:)
├─config.txt
├─LOG.TXT
├─ MB/
│   └─ HBI0262?/
│        ├─ mbb_v???.ebf
│        ├─ board.txt
│        ├─ io_v?.ebf
│        ├─ pms_v?.bin
│        └─ tapid.arm
├─ SITE1/
│   └─ HBI0262?/
│        ├─ board.txt
│        └─ images.txt
├─ SITE2/
│   └─ HBI0????/
│        ├─dbb_v???.ebf
│        ├─ board.txt
│        ├─ AN???
│        ¦    ├─an???_v?.rbf
│        ¦    ├─an???_v?.txt
│        ¦    └─images.txt
│        ▼
└─SOFTWARE/
    ├─bl1.bin
    ├─fip.bin
    ├─ Image
    └─juno.dtb
```

Figure 3-3 Example configuration microSD card directory structure

The directory structure and file name format ensure that each image is matched to the correct target device defined in the V2M-Juno r2 motherboard configuration EEPROM and in the daughterboard EEPROM.

`config.txt`
: Generic configuration file for all motherboards. This file applies to all Versatile Express motherboards including the V2M-Juno r2 motherboard.

`MB` directory
: Contains subdirectories for any motherboard variants present in the system. The subdirectory names match the HBI codes for the specific motherboard variants. The files in these directories contain clock, register, and other settings for the boards.

`SITE1` directory
: Contains configuration files that relate to the Juno r2 SoC and to external memory that the Juno r2 SoC can access.

`SITE2` directory
: Contains configuration files for any LogicTile daughterboard that you fit to the V2M-Juno r2 motherboard. The subdirectory names match the HBI codes for all possible daughterboards. The files in these directories contain clock, register, and other settings for the daughterboards.

`SOFTWARE` directory
: Contains application files that the MCC can load into SRAM or NOR flash. The `IMAGES` section in the `config.txt` file defines the file that the MCC loads.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.
1.4 Connectors on front and rear panels on page 1-16.
A.2 Configuration 10Mbps Ethernet and dual-USB connector on page Appx-A-125.
A.5 Configuration USB connector on page Appx-A-128.

3.3.2 `config.txt` generic motherboard configuration file

You can use the V2M-Juno r2 motherboard configuration USB port or configuration Ethernet port to update the generic Versatile Express configuration file `config.txt` from your workstation to the root directory of the microSD card.

The following example shows a typical `config.txt` configuration file in the root directory of the configuration microSD card.

Note

- Colons (:) indicate the end of commands and must be separated by a space character (`0x20`) from the value fields.
- Semicolons (;) indicate comments.
- *`ASSERTNPOR`* must always have the value TRUE.

```
TITLE: Versatile Express V2M-Juno configuration file

[CONFIGURATION]
AUTORUN: FALSE                ;Auto Run from power on
TESTMENU: FALSE               ;MB Peripheral Test Menu

UPDATE: FALSE                 ;Force JTAG and FPGA update to DBs
VERIFY: FALSE                 ;Force FPGA verify to DBs

DVIMODE: VGA                  ;VGA or SVGA or XGA or SXGA or UXGA

MBLOG: FALSE                  ;LOG MB MICRO in run mode FALSE/UART0/UART1
DBLOG: FALSE                  ;LOG DB MICRO in run mode FALSE/UART1
                              ;(when MBLOG is not UART1)

USERSWITCH: 00000000          ;Userswitch[7:0] in binary
CONFSWITCH: 00000000          ;Configuration Switch[7:0] in binary
ASSERTNPOR: TRUE              ;External resets assert nPOR
WDTRESET: NONE                ;Watchdog reset options NONE/RESETMB/RESETDB

PCIMASTER: DB1                ;Port Failover DB1/SL3
MASTERSITE: DB1               :Boot Master DB1/SL3
REMOTE: NONE                  ;Selects remote command options NONE/USB/FTP

SMCMACADDRESS: 0xFFFFFFFFFFFF ;MAC Address for SMC Ethernet
MCCMACADDRESS: 0xFFFFFFFFFFFF ;MAC Address for MCC configuration Ethernet

HOSTNAME: V2M_JUNO_01         ;Host name for FTP [15 characters max]
```

See *2.13 UART interface* on page 2-52 for information on using the *`MBLOG`* and *`DBLOG`* options to configure the UART interface.

3.3.3 Contents of the `MB` directory

The `MB` directory contains files that relate to the MCC and to other components on the V2M-Juno r2 motherboard, but not the Juno r2 SoC. The `MB` directory contains a configuration HBI subdirectory that matches the HBI code of the V2M-Juno r2 motherboard.

The HBI subdirectory contains the following:

A `board.txt` file	Defines the BIOS image that the MCC loads during configuration.
A file of the form `mbb_vxxx.ebf`.	MCC BIOS image that the `board.txt` file defines.
A file of the form `io_bxxx.bit`	IOFPGA image file.

A file of the form `pms_vxxx.bin`	Binary configuration file for the *Power Management IC* (PMIC) on the V2M-Juno r2 motherboard.
A `tapid.arm` file	Contains JTAG ID codes for the V2M-Juno r2 motherboard and LogicTile daughterboards.

The following example shows a typical V2M-Juno r2 motherboard configuration `board.txt` file.

```
BOARD: HBI0262
TITLE: Motherboard configuration file

[MCCS]
MBBIOS mbb_v117.ebf                 ;MB BIOS IMAGE

[FPGAS]
MBIOFPGA: io_v114.bit               ;MB IOFPGA

[PMIC]
MBPMIC: pms_v103.bin                ;MB PMIC

[OSCCLKS]
TOTALOSCCLKS: 11
OSC0: 50.0                          ;OSC0 Juno SYSREFCLK    (System clock)
OSC1: 50.0                          ;OSC1 Juno AONREFCLK    (Always on)
OSC2: 50.0                          ;OSC2 Juno PXLREFCLK    (HS pixel clock)
OSC3: 50.0                          ;OSC3 Juno PXLCLKIN     (LS pixel clock)
OSC4: 2.11                          ;OSC4 Juno I2SCLK       (Audio)
OSC5: 50.0                          ;OSC5 Juno SMCMCLK      (Static memory)
OSC6: 50.0                          ;OSC6 Juno CA53_REF_CLK (RSVD)
OSC7: 50.0                          ;OSC7 Juno CA72_REF_CLK (RSVD)
OSC8: 50.0                          ;OSC8 Juno GPU_REF_CLK  (RSVD)
OSC9: 50.0                          ;OSC9 IOFPGA BOOT       (RSVD)
OSC10: 24.0                         ;OSC10 IOFPGA UART      (RSVD)
OSC11: 7.37                         ;OSC11 Juno UARTCLK     (UART clock)
```

Related concepts

2.5.1 Overview of clocks on page 2-28.

3.3.4 Contents of the `SITE1` directory

The `SITE1` directory contains files that relate to the Juno r2 SoC and to external memory on the V2M-Juno r2 motherboard that the Juno r2 SoC can access.

The `SITE1` subdirectory contains an `HBI0262D` subdirectory that matches the HBI code of the V2M-Juno r2 motherboard. The `HBI0262D` subdirectory contains the following files:

A `board.txt` file

Contains configuration information for the SCC registers in the Juno r2 SoC.

An `images.txt` file

Defines the files that the MCC loads into external memory during configuration.

The following example shows a typical V2M-Juno r2 motherboard `board.txt` file in the `SITE1` directory that relates to the Juno r2 SoC.

```
BOARD: HBI0262
TITLE: V2M-Juno DevChip Configuration File

[SCC REGISTERS]
TOTALSCCS: 7                    ;Total Number of SCC registers
SCC: 0x100 0x801F1000           ;A72 PLL Register 0 (800MHz)
SCC: 0x104 0x0000F100           ;A72 PLL Register 1
SCC: 0x108 0x801B1000           ;A53 PLL Register 0 (700MHz)
SCC: 0x10C 0x0000D100           ;A53 PLL Register 1
SCC: 0x0F8 0x0BEC0000           ;BL1 entry point
```

Caution

ARM reserves these registers. You must not write to them.

The following example shows a typical V2M-Juno r2 motherboard `images.txt` file in the `SITE1` directory that relates to the Juno r2 SoC.

```
TITLE: Versatile Express Images Configuration File

[IMAGES]
TOTALIMAGES: 4                       ;Number of Images (Max : 32)

NOR0UPDATE: AUTO                     ;Image Update:NONE/AUTO/FORCE
NOR0ADDRESS: 0x00000000              ;Image Flash Address
NOR0FILE: \SOFTWARE\fip.bin          ;Image File Name
NOR0LOAD: 00000000                   ;Image Load Address
NOR0ENTRY: 00000000                  ;Image Entry Point

NOR1UPDATE: AUTO                     ;Image Update:NONE/AUTO/FORCE
NOR1ADDRESS: 0x03EC0000              ;Image Flash Address
NOR1FILE: \SOFTWARE\bl1.bin          ;Image File Name
NOR1LOAD: 00000000                   ;Image Load Address
NOR1ENTRY: 00000000                  ;Image Entry Point

NOR2UPDATE: AUTO                     ;Image Update:NONE/AUTO/FORCE
NOR2ADDRESS: 0x00500000              ;Image Flash Address
NOR2FILE: \SOFTWARE\Image            ;Image File Name
NOR2LOAD: 00000000                   ;Image Load Address
NOR2ENTRY: 00000000                  ;Image Entry Point

NOR3UPDATE: AUTO                     ;Image Update:NONE/AUTO/FORCE
NOR3ADDRESS: 0x00F00000              ;Image Flash Address
NOR3FILE: \SOFTWARE\juno.dtb         ;Image File Name
NOR3LOAD: 00000000                   ;Image Load Address
NOR3ENTRY: 00000000                  ;Image Entry Point
```

3.3.5 Contents of the `SITE2` directory

The `SITE2` directory contains configuration files for LogicTile daughterboards that you can fit in the V2M-Juno r2 motherboard daughterboard site.

See the Technical Reference Manual for your fitted daughterboard for information about the daughterboard files in the `SITE2` directory.

3.3.6 Contents of the `SOFTWARE` directory

The `SOFTWARE` directory contains applications that you can load into external flash memory.

You can create new applications and load them into the flash memory on the V2M-Juno r2 motherboard. Application images are typically boot images or demo programs and have a `.axf` extension.

Typical applications in this directory are:
- `bl1.bin` ARM Trusted Firmware.
- `fip.bin` Firmware Image Package that contains BL2, $BL3_0$, $BL3_1$, $BL3_3$.
- `Image` Linux kernel.
- `juno.dtb` Juno device tree.

3.4 Configuration switches

The V2M-Juno r2 motherboard provides configuration switches, SW0 and SW1.

This section contains the following subsections:
- *3.4.1 Use of configuration switches* on page 3-75.
- *3.4.2 Remote UART configuration* on page 3-75.

3.4.1 Use of configuration switches

The SW0 and SW1 switches affect board initialization.

The `config.txt` configuration file contains *`USERSWITCH`* and *`CFGSWITCH`* entries for the virtual switch register bits SYS_SW[7:0] and SYS_CFGSW[7:0] in the IOFPGA. Configuration switch SW0 also modifies SYS_SW[0]. The configuration system does not use these virtual switches for system configuration, but they are available for the user application and boot monitor.

See the following for more information:

- *4.3.3 SYS_SW Register* on page 4-90.
- *4.3.7 SYS_CFGSW Register* on page 4-93.

Note

- The default setting for configuration switches SW0 and SW1 is OFF.
- If the switches are in the up position, they are OFF.

Bootscript switch SW0

SW0 in the ON position, or the `config.txt` entry for USERSWITCH[0] being set to 1, sets SYS_SW[0] to `0b1`.

If SYS_SW[0] is set to `0b1`, the boot loader runs the OS automatically at powerup. If the OS software supports this feature, under UEFI, this boot process starts automatically irrespective of the switch setting.

SYS_SW[30] indicates the value of physical configuration switch SW0.

A user application can also modify SYS_SW[0] but the change does not take effect until the next reset.

Remote UART control switch SW1

SW1 in the ON position enables UART control and the flow-control signals on UART0 to control the standby-state. This setting is typically used on test farms.

SYS_SW[31] indicates the value of physical configuration switch SW1.

See the following for the location of the configuration switches:
- *1.3 Location of components on the V2M-Juno r2 motherboard* on page 1-15.
- *1.4 Connectors on front and rear panels* on page 1-16.

3.4.2 Remote UART configuration

If SW1 is ON, to enable remote UART control:

- An external controller can toggle UART0 **SER0_DSR**, pin 6, HIGH for 100ms to put the V2M-Juno r2 motherboard into standby-state. This is equivalent to pressing the *Hardware Reset* button. Power cycling the board also places the system in standby-state.

Note

The duration of the **SER0_DSR** HIGH pulse must be greater than or equal to 100ms.

- An external controller can remotely select whether the MCC or the system application uses UART0 in run-mode. This overrides the `confix.txt` entry for MBLOG and eliminates the requirement to use the second serial port on UART1.

  Set UART0 **SER0_CTS**, pin 8, LOW to select system mode, or set it HIGH to select MCC mode.

  Remote UART0 control requires a full null modem cable that ARM supplies with the V2M-Juno r2 motherboard. The following figure shows the cable wiring.

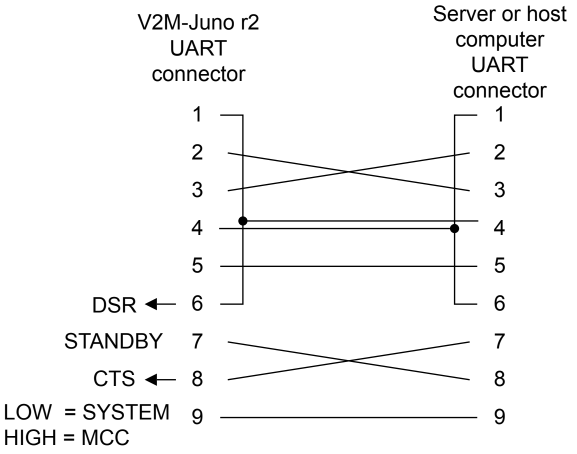


Figure 3-4 Modem cable wiring

You can control the **SER0_DSR** and **SER0_CTS** signals using control logic on the host computer.

Alternatively, you can use a custom terminal program such as `ARM VETerminal.exe` that ARM provides on the V2M-Juno r2 motherboard DVD. This program integrates the terminal output and control buttons into a single application.

3.5 Use of reset push buttons

The ON/OFF/Soft Reset button performs a software reset of the system, and the Hardware Reset button performs a hardware reset of the system.

This section contains the following subsections:

- *3.5.1 Use of ON/OFF/Soft Reset button* on page 3-77.
- *3.5.2 Use of Hardware Reset button* on page 3-77.

3.5.1 Use of ON/OFF/Soft Reset button

This push button enables you to perform a software reset of the system.

You initiate a software reset of the system by briefly pressing the *ON/OFF/Soft Reset* button during run time. The MCC performs a software reset of the Juno r2 SoC and resets the devices on the board.

The software reset sequence is as follows:

1. Briefly press the *ON/OFF/Soft Reset* button.

   Caution

   If you press and hold the *ON/OFF/Soft Reset* button for more than two seconds, the system enters the standby-state in the same way as pressing the *Hardware Reset* button.

2. The MCC asserts the **CB_nRST** reset signal.
3. The MCC releases **CB_nPOR**.
4. The MCC releases **CB_nRST**.
5. The V2M-Juno r2 motherboard enters the operating-state.

Note

- The MCC does not read the configuration files or perform a board reconfiguration as a result of a software reset.
- The **CB_nPOR** signal drives the **nPORESET** signal inside the Juno r2 SoC.

Related concepts

2.6.1 Reset push buttons on page 2-35.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

3.5.2 Use of Hardware Reset button

This push button enables you to perform a hardware reset of the system.

You can change the operation of the board from the operating-state to the standby-state by briefly pressing the *Hardware Reset* button. This switches off the power to the board and resets the system to the default values.

If you then press the *ON/OFF/Soft Reset* push button, the system performs a full configuration and enters the operating-state.

Related concepts

2.6.1 Reset push buttons on page 2-35.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

3.6 Command-line interface

The V2M-Juno r2 motherboard command-line interface supports system command-line input to the MCC and to the Daughterboard Configuration Controller on the LogicTile daughterboard.

This section contains the following subsections:

- *3.6.1 Overview of the V2M-Juno r2 motherboard MCC command-line interface* on page 3-78.
- *3.6.2 Overview of the LogicTile daughterboard command-line interface* on page 3-78.
- *3.6.3 MCC main command menu* on page 3-78.
- *3.6.4 MCC debug menu* on page 3-79.
- *3.6.5 EEPROM menu* on page 3-79.

3.6.1 Overview of the V2M-Juno r2 motherboard MCC command-line interface

You must connect a workstation to UART0 to enter MCC system commands.

You must set the *`MBLOG`* option in the `config.txt` to `TRUE` to enter MCC system commands at the UART0 port.

The workstation settings must be:

- 115.2kBaud.
- 8N1 representing 8 data bits, no parity, one stop bit.
- No hardware or software flow control.

3.6.2 Overview of the LogicTile daughterboard command-line interface

You must connect a workstation to UART1 to input system commands to the Daughterboard Configuration Controller on the LogicTile daughterboard.

You must set the *`DBLOG`* option in the `config.txt` to `TRUE` to enter LogicTile daughterboard system commands at the UART1 port. The setting takes effect after the next reset.

The workstation settings must be:

- 115.2kBaud.
- 8N1 representing 8 data bits, no parity, one stop bit.
- No hardware or software flow control.

See the appropriate Technical Reference Manual for your LogicTile daughterboard for information on the daughterboard command-line interface.

3.6.3 MCC main command menu

The following table shows the MCC main menu system commands.

Table 3-1 V2M-Juno r2 motherboard MCC main command menu

Command	Description
`CAP` *`filename`* `[/A]`	Capture serial data to the file *`filename`*. Use the `/A` option to append data to an existing file.
`COPY` *`input_filename_1`* `[`*`input_filename_2`*`]` *`output_filename`*	Copy a file *`input_filename_1`* to *`output_filename`*. Option *`input_filename_2`* merges *`input_filename_1`* and *`input_filename_2`*.
`DEBUG`	Change to the debug menu.
`DEL` *`filename`*	Delete file *`filename`*.
`DIR [`*`mask`*`]`	Display a list of files in the directory.
`EEPROM`	Change to the EEPROM menu.

Table 3-1 V2M-Juno r2 motherboard MCC main command menu (continued)

Command	Description
`FILL` *filename* [*nnnn*]	Create a file *filename* filled with text. *nnnn* specifies the number of lines to create. The default is 1000.
`FTP_ON`	Enable MCC FTP Server.
`FTP_OFF`	Disable MCC FTP Server.
`HELP` or `?`	Display this help.
`REBOOT`	Cycle system power and reboot.
`RECAL`	Calibrate the PVT sensor.
`REN` *filename_1 filename_2*	Rename a file from *filename_1* to *filename_2*.
`RESET`	Reset the V2M-Juno r2 motherboard using the **nRST** reset signal.
`SHUTDOWN`	Shutdown the power supply but leave the MCC running. The board returns to Standby mode.
`TYPE` *filename*	Display the contents of text file *filename*.
`USB_ON`	Enable MCC USB configuration port.
`USB_OFF`	Disable MCC USB configuration port.

3.6.4 MCC debug menu

Enter `DEBUG` at the main menu to switch to the debug submenu. The debug submenu is valid only in operating-state.

The following table shows the debug commands.

Table 3-2 V2M-Juno r2 motherboard MCC debug command menu

Command	Description
`DATE`	Display current date.
`DEBUG [0|1]`	Enable or disable debug printing: `0b0` Disable. `0b1` Enable.
`DEPOSIT` *address data*	Write word to system memory address.
`EXAM` *address* [*nnnn*]	Examine system memory address at *address*. *nnnn* is number, in Hex, of words to read.
`EXIT` or `QUIT`	Return to main menu.
`HELP` or `?`	Display this help.
`TIME`	Display current time.

3.6.5 EEPROM menu

Enter `EEPROM` at the main menu to switch to the EEPROM submenu. The contents of the V2M-Juno r2 motherboard EEPROMs identify the specific board variant and might contain data to load to the other devices on the board.

The following table shows the EEPROM commands.

Caution

You must not modify the EEPROM settings. The settings are programmed with unique values during production and changing them might compromise the function of the board.

Table 3-3 V2M-Juno r2 motherboard EEPROM commands

Command	Description
`CONFIG 0` *`filename`*	Write configuration file to EEPROM.
`EXIT` or `QUIT`	Return to main menu.
`ERASECON [0]`	Erase configuration section of EEPROM.
`ERASEDEV [0]`	Erase device section of EEPROM.
`ERASERANGE [0]` *`start end`*	Erase EEPROM between *`start`* and *`end`*.
`ERASEIMAGE` *`image_id`*	Erase image, named *`image_id`*, stored in Motherboard EEPROM.
`ERASEIMAGES`	Erase images stored in Motherboard EEPROM.
`HELP` or `?`	Display this help.
`READIMAGES`	Read images stored in Motherboard EEPROM.
`READCF [0]`	Read configuration EEPROM.
`READRANGE [0]` [*`start`*] [*`end`*]	Read EEPROM between *`start`* and *`end`*.

Chapter 4

Programmers Model

This chapter describes the programmers model of the Versatile Express V2M-Juno r2 motherboard.

It contains the following sections:

4.1 About this programmers model

The Juno r2 SoC programmers model derives from the ARMv8-A compute subsystem architecture that supports ARMv8-A AARch64 software and tooling.

The following information applies to the SCC registers and to the system configuration, SYS_CFG, registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or powerup reset.
  - *4.3.1 APB system register summary* on page 4-88, *4.4.1 APB system configuration register summary* on page 4-102, and *4.5.1 APB energy register summary* on page 4-106 describe register access type as follows:

RW	Read and write.
RO	Read-only.
WO	Write-only.

4.2 V2M-Juno r2 motherboard memory maps

The application processors in the Juno r2 SoC on the V2M-Juno r2 motherboard see a 40-bit memory map.

This section contains the following subsections:

- *4.2.1 Juno r2 SoC top-level application and SMC interface memory maps* on page 4-83.
- *4.2.2 IOFPGA system peripherals memory map* on page 4-84.
- *4.2.3 DDR3L memory map* on page 4-86.
- *4.2.4 Additional Juno r2 SoC memory maps* on page 4-87.

4.2.1 Juno r2 SoC top-level application and SMC interface memory maps

The Juno r2 SoC SMC occupies the expansion AXI memory at `0x0008000000` and supports chip-selects that access components, systems, and memory on the V2M-Juno r2 motherboard. The security status is exported security.

Chip select CS3 inside the SMC accesses the low-bandwidth system peripherals inside the IOFPGA and is at `0x001C000000`.

The following figure shows the mapping of the SMC memory map into the Juno r2 SoC top-level application memory map.

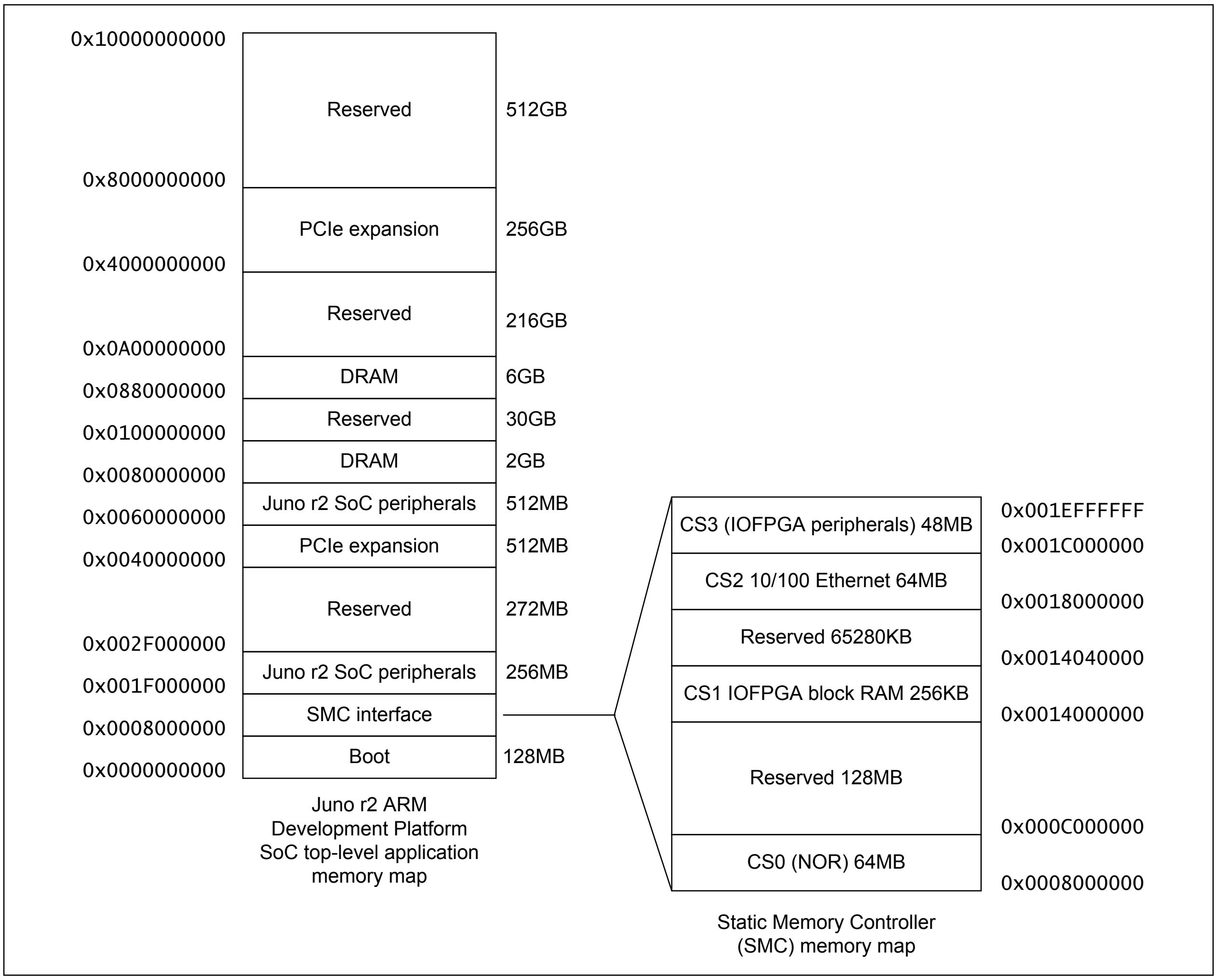


Figure 4-1 Juno r2 SoC top-level application and SMC interface memory maps

The following table shows the SMC memory map of the V2M-Juno r2 motherboard.

Table 4-1 SMC interface memory map of V2M-Juno r2 motherboard

Address range	Size	Description
`0x08000000-0x0BFFFFFF`	64MB	CS0-Motherboard NOR flash.
`0x0C000000-0x13FFFFFF`	128MB	Reserved. Do not write to or read from these addresses.
`0x14000000-0x1403FFFF`	256KB	CS1-256KB internal IOFPGA block RAM.
`0x14040000-0x17FFFFFF`	65280KB	Reserved. Do not write to or read from these addresses.
`0x18000000-0x1BFFFFFF`	64MB	CS2-10/100 Ethernet.
`0x1C000000-0x1EFFFFFF`	48MB	CS3-IOFPGA peripherals.

See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* for more information.

4.2.2 IOFPGA system peripherals memory map

The memory map of the IOFPGA system peripherals is at chip select CS3 in the SMC interface.

The chip select CS3 is at `0x001C000000` and provides access to low-bandwidth system peripherals in the IOFPGA that the Juno r2 SoC does not provide.

The following figure shows the mapping of the IOFPGA system peripherals memory map into the SMC memory map.

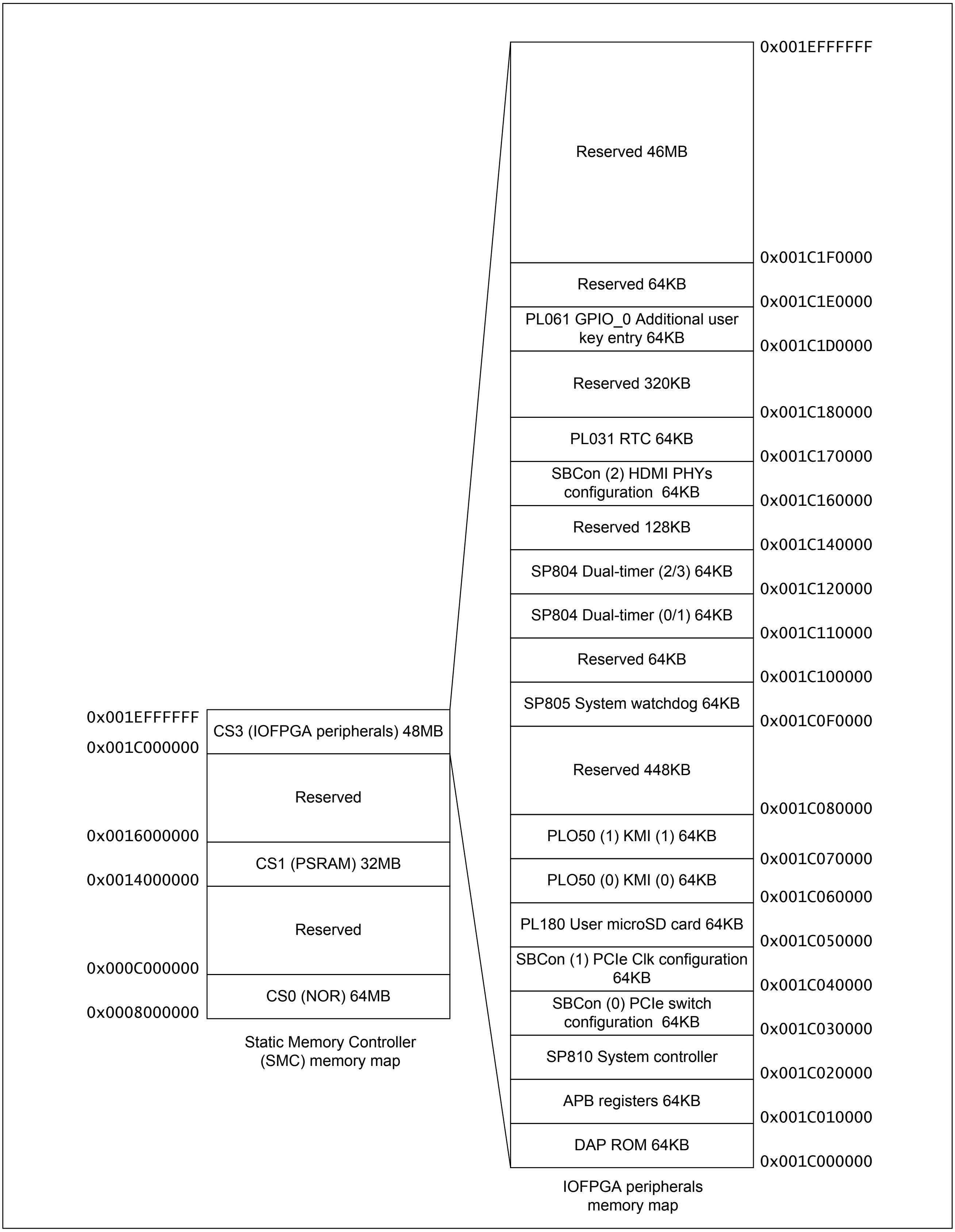


Figure 4-2 V2M-Juno r2 motherboard IOFPGA system peripherals memory map

The following table shows the IOFPGA system peripherals memory map.

Table 4-2 V2M-Juno r2 motherboard IOFPGA system peripherals memory map

Address range	Size	Description
`0x1C000000-0x1C00FFFF`	64KB	CS3-DAP ROM.
`0x1C010000-0x1C01FFFF`	64KB	CS3-APB registers.
`0x1C020000-0x1C02FFFF`	64KB	CS3-SP810 System controller.
`0x1C030000-0x1C03FFFF`	64KB	CS3-SBCon (0). PCIe switch I^2C.
`0x1C040000-0x1C04FFFF`	64KB	CS3-SBCon (1). PCIe clock configuration.
`0x1C050000-0x1C05FFFF`	64KB	CS3-PL180 User microSD card.
`0x1C070000-0x1C07FFFF`	64KB	CS3-PL050 (1) KMI interface 1.
`0x1C080000-0x1C0EFFFF`	448KB	Reserved. Do not write to or read from these addresses.
`0x1C0F0000-0x1C0FFFFF`	64KB	SP805 System watchdog.
`0x1C100000-0x1C1FFFFF`	64KB	Reserved. Do not write to or read from these addresses.
`0x1C110000-0x1C11FFFF`	64KB	CS3-SP804 Dual-timer (0/1).
`0x1C120000-0x1C12FFFF`	64KB	CS3-SP804 Dual-timer (2/3).
`0x1C140000-0x1C15FFFF`	128KB	Reserved. Do not write to or read from these addresses.
`0x1C160000-0x1C16FFFF`	64KB	CS3-SBCon (2). HDMI PHYs configuration.
`0x1C170000-0x1C17FFFF`	64KB	PL031 RTC.
`0x1C180000-0x1C1CFFFF`	320KB	Reserved. Do not write to or read from these addresses.
`0x1C1D0000-0x1C1DFFFF`	64KB	CS3-PL061 GPIO 0 Additional user key entry.
`0x1C1E0000-0x1C1EFFFF`	64KB	Reserved. Do not write to or read from these addresses.
`0x1C1F0000-0x1EFFFFFF`	46MB	Reserved. Do not write to or read from these addresses.

Related concepts

2.8 IOFPGA on page 2-42.

4.2.3 DDR3L memory map

The DDR3L memory map occupies two parts of the Juno r2 SoC top-level application map, 2GB at `0x0080000000`, and 6GB at `0x0880000000`. The security is programmable access security.

The following figure shows the mapping of the DDR3L memory map into the Juno r2 SoC top-level application memory map.

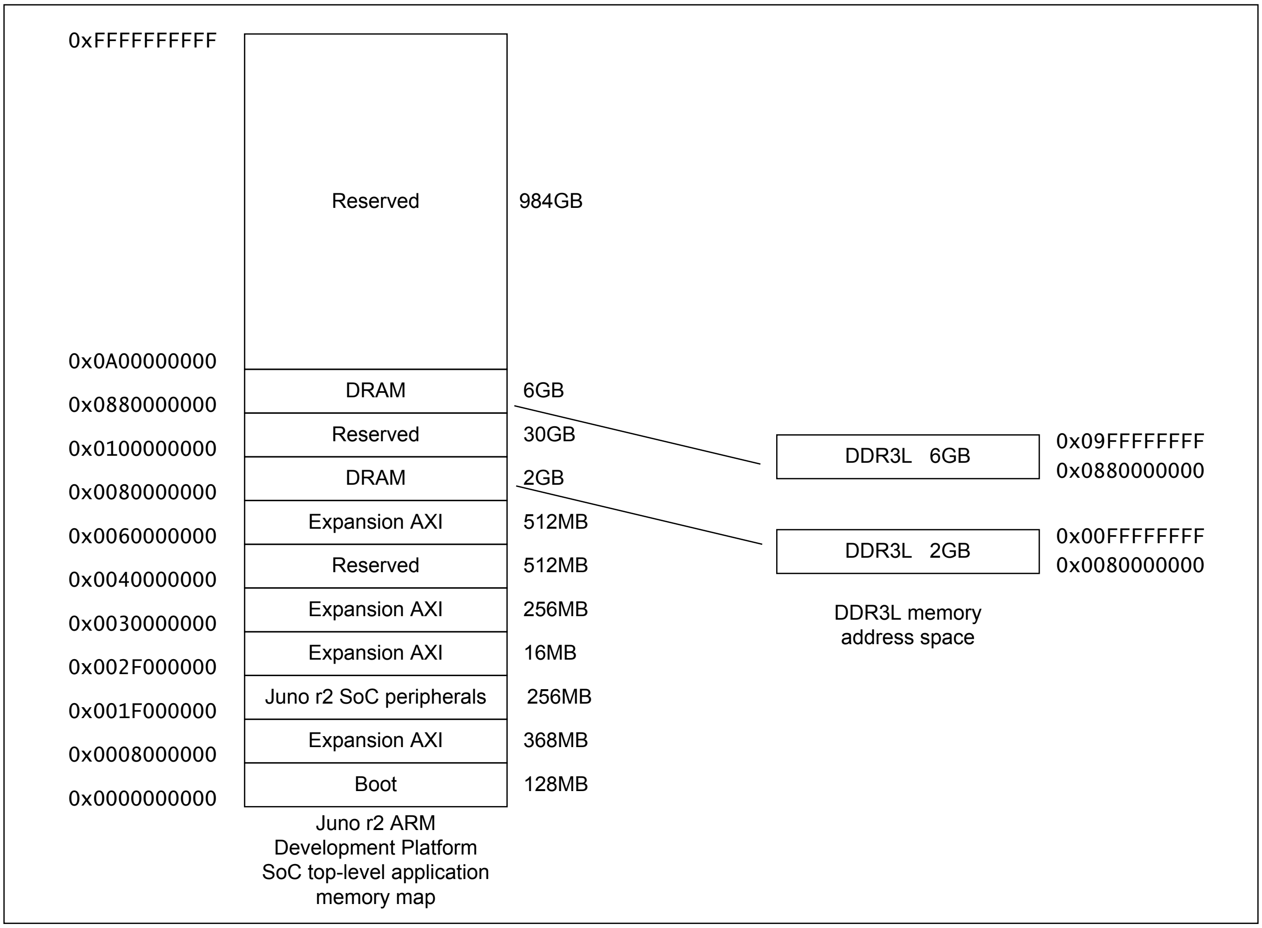


Figure 4-3 V2M-Juno r2 motherboard DDR3L memory map

The following table shows the V2M-Juno r2 motherboard DDR3L memory map.

Table 4-3 V2M-Juno r2 motherboard DDR3L memory map

Address range	Size	Description
`0x0080000000-0x00FFFFFFFF`	2GB	DDR3L
`0x0880000000-0x09FFFFFFFF`	6GB	DDR3L

4.2.4 Additional Juno r2 SoC memory maps

The Juno r2 SoC contains additional memory maps.

See the *Juno ARM® Development Platform SoC Technical Reference Manual (Revision r2p0)* for information on other areas of the top-level memory map of the Juno r2 SoC.

4.3 APB system registers

The IOFPGA contains the APB system registers.

This section contains the following subsections:

4.3.1 APB system register summary

The base memory address of the APB system registers in the IOFPGA is `0x1C010000`

The following table shows the registers in address offset order from the base memory address.

Table 4-4 V2M-Juno r2 motherboard APB system register summary

Offset	Name	Type	Reset	Width	Description
`0x0000`	SYS_ID	RO	`0xXXXXXXXX`	32	See *4.3.2 SYS_ID Register* on page 4-89.
`0x0004`	SYS_SW	RO/RW	`0xX00000XX`	32	See *4.3.3 SYS_SW Register* on page 4-90.
`0x0008`	SYS_LED	RO/RW	`0x000000XX`	32	See *4.3.4 SYS_LED Register* on page 4-91.
`0x0024`	SYS_100HZ	RO/RW	`0xXXXXXXXX`	32	See *4.3.5 SYS_100HZ Register* on page 4-92.
`0x0030`	SYS_FLAG	RO	`0x00000000`	32	See *4.3.6 SYS_FLAG Registers* on page 4-92.
`0x0030`	SYS_FLAGSSET	WO	-	32	See *4.3.6 SYS_FLAG Registers* on page 4-92
`0x0034`	SYS_FLAGSCLR	WO	-	32	See *4.3.6 SYS_FLAG Registers* on page 4-92.
`0x0038`	SYS_NVFLAGS	RO	`0x00000000`	32	See *4.3.6 SYS_FLAG Registers* on page 4-92.
`0x0038`	SYS_NVFLAGSSET	WO	-	32	See *4.3.6 SYS_FLAG Registers* on page 4-92.
`0x003C`	SYS_NVFLAGSCLR	WO	-	32	See *4.3.6 SYS_FLAG Registers* on page 4-92.
`0x0058`	SYS_CFGSW	RO/RW	`0x000000XX`	32	See *4.3.7 SYS_CFGSW Register* on page 4-93.

Table 4-4 V2M-Juno r2 motherboard APB system register summary (continued)

Offset	Name	Type	Reset	Width	Description
`0x005C`	SYS_24MHZ	RO	`0xXXXXXXXX`	32	See *4.3.8 SYS_24MHZ Register* on page 4-94.
`0x0060`	SYS_MISC	RW/RO	`0x00000000`	32	See *4.3.9 SYS_MISC Register* on page 4-95.
`0x0070`	SYS_PCIE_CNTL	RW	`0x0000000X`	32	See *4.3.10 SYS_PCIE_CNTL Register* on page 4-95.
`0x0074`	SYS_PCIE_GBE_L	RO	`0xXXXXXXXX`	32	See *4.3.11 SYS_PCIE_GBE Register* on page 4-96.
`0x0078`	SYS_PCIE_GBE_H	RO	`0x0000XXXX`	32	See *4.3.11 SYS_PCIE_GBE Register* on page 4-96.
`0x0084`	SYS_PROC_ID0	RW	`0x0X000000`	32	See *4.3.12 SYS_PROC_ID0 Register* on page 4-97.
`0x0088`	SYS_PROC_ID1	RW	`0x0X000XXX`	32	See *4.3.13 SYS_PROC_ID1 Register* on page 4-97.
`0x0120`	SYS_FAN_SPEED	RW	`0x00000000`	32	See *4.3.14 SYS_FAN_SPEED Register* on page 4-98.

The base memory address of the SP810 system control register is `0x1C020000`. The following table shows the SP810 system control register.

Offset	Name	Type	Reset	Width	Comment
`0x0000`	SP810_CTRL	RW	`0x00000000`	32	See *4.3.15 SP810_CTRL Register* on page 4-99.

4.3.2 SYS_ID Register

The SYS_ID Register characteristics are:

Purpose

Contains information about the V2M-Juno r2 motherboard and the bus and image versions inside the IOFPGA.

Usage constraints

The SYS_ID Register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

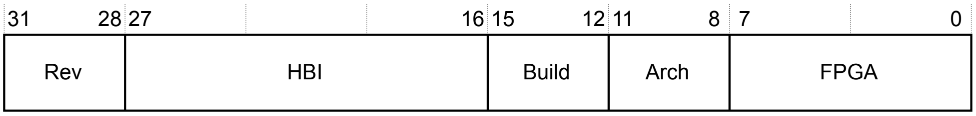


Figure 4-4 SYS_ID Register bit assignments

The following table shows the bit assignments.

Table 4-5 SYS_ID Register bit assignments

Bits	Name	Function
[31:28]	Rev	Board revision: `0x0` Rev A board. This is the prototype board and contains the Juno r0 SoC. `0x1` Rev B board. This board contains the Juno r0 SoC. `0x2` Rev C board. This board contains the Juno r1 SoC. `0x3` Rev D board. This board contains the Juno r2 SoC.
[26:16]	HBI	HBI board number in BCD: `0x262` HBI0262.
[15:12]	Build	Build variant of board: `0xF` All builds.
[11:8]	Arch	IOFPGA bus architecture: `0x4` AHB. `0x5` AXI.
[7:0]	FPGA	FPGA build in BCD. The actual value that is read depends on the FPGA build.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.3 SYS_SW Register

The SYS_SW Register characteristics are:

Purpose
Reads the *`USERSWITCH`* entry in the `config.txt` file. A bit set to `0b1` indicates that the switch is ON.

Usage constraints
Bits[31:8] are read-only. Bits[7:0] are read-write.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

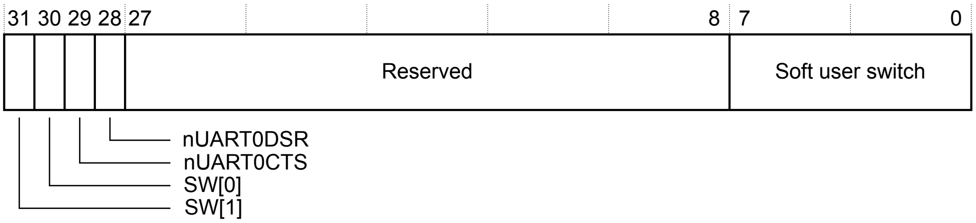


Figure 4-5 SYS_SW Register bit assignments

The following table shows the bit assignments.

Table 4-6 SYS_SW Register bit assignments

Bits	Name	Function
[31]	SW[1]	Indicates the value of the physical configuration switch SW[1]: `0b1` ON.
[30]	SW[0]	Indicates the value of the physical configuration switch SW[0]: `0b1` ON.
[29]	nUART0CTS	UART0 CTS signal.
[28]	nUART0DSR	UART0 DSR signal.
[27:8]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[7:0]	Soft user switch.	Application software can read these switch settings. If SYS[0] = `0b1`, the Boot Monitor runs its bootscript at powerup.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.4 SYS_LED Register

The SYS_LED Register characteristics are:

Purpose
Controls the eight user LEDs on the V2M-Juno r2 motherboard. All LEDs are turned OFF at reset. The Boot Monitor updates the LED value.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

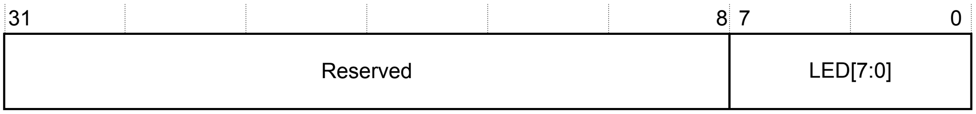


Figure 4-6 SYS_LED Register bit assignments

The following table shows the bit assignments.

Table 4-7 SYS_LED Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[7:0]	LED[7:0]	Set or read the user LED states: `0b0` OFF. `0b1` ON.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.5 SYS_100HZ Register

The SYS_100HZ Register characteristics are:

Purpose
A 32-bit counter that updates at 100Hz. The input clock derives from the 24MHz clock generator on the V2M-Juno r2 motherboard.

Usage constraints
The SYS_100HZ Register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

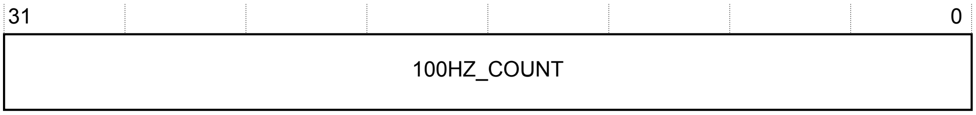


Figure 4-7 SYS_100HZ Register bit assignments

The following table shows the bit assignments.

Table 4-8 SYS_100HZ Register bit assignments

Bits	Name	Function
[31:0]	100HZ_COUNT	Contains the count, at 100Hz, since the last **CB_nRST** reset.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.6 SYS_FLAG Registers

The SYS_FLAG Registers characteristics are:

Purpose
Provide two 32-bit registers, SYS_FLAGS and SYS_NVFLAGS, that contain general-purpose flags. The application software defines the meaning of the flags. You use the SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET, and SYS_NVFLAGSCLR registers to set and clear the bits in the Flag Registers.

Usage constraints

The SYS_FLAGS and SYS_NVFLAGS Registers are read-only.

The SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET, and SYS_NVFLAGSCLR Registers are write-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

SYS_FLAGS Register

The SYS_FLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_FLAGS Register is volatile, that is, a reset signal from the reset push button resets the SYS_FLAGS Register.

You use the SYS_FLAGSSET Register to set bits in the SYS_FLAGS Register. Write `0b1` to set the associated flag. Write `0b0` to leave the associated flag unchanged.

You use the SYS_FLAGSCLR Register to clear bits in the SYS_FLAGS Register. Write `0b1` to clear the associated flag. Write `0b0` to leave the associated flag unchanged.

SYS_NVFLAGS Register

The SYS_NVFLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_NVFLAGS Register is non-volatile, that is, a reset signal from the reset push button does not reset the SYS_FLAGS Register. Only **CB_nPOR** resets the SYS_NVFLAGS Register.

You use the SYS_NVFLAGSSET Register to set bits in the SYS_NVFLAGS Register. Write `0b1` to set the associated flag. Write `0b0` to leave the associated flag unchanged.

You use the SYS_NVFLAGSCLR Register to clear bits in the SYS_NVFLAGS Register. Write `0b1` to clear the associated flag. Write `0b0` to leave the associated flag unchanged.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.7 SYS_CFGSW Register

The SYS_CFGSW Register characteristics are:

Purpose

Contains the value of *`CONFSWITCH`* in the `config.txt` file.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

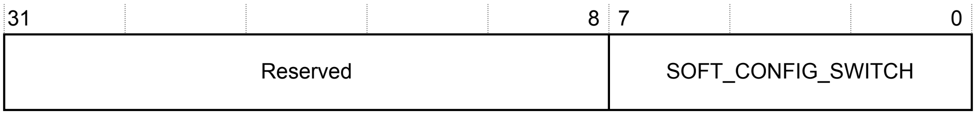


Figure 4-8 SYS_CFGSW Register bit assignments

The following table shows the bit assignments.

Table 4-9 SYS_CFGSW Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[7:0]	SOFT_CONFIG_SWITCH	Software applications can read these switch settings. The application software defines the meanings of the switch settings. The reset signals set these bits to the value of *`CONFSWITCH`* in the `config.txt` file. **Note** The configuration system does not use the contents of this register for board configuration.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.8 SYS_24MHZ Register

The SYS_24MHZ Register characteristics are:

Purpose
A 32-bit counter that updates at 24MHz. The clock source is the 24MHz clock generator on the V2M-Juno r2 motherboard.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

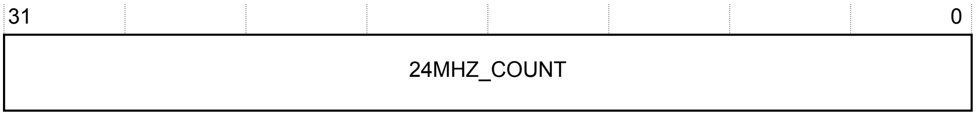


Figure 4-9 SYS_24MHZ Register bit assignments

The following table shows the bit assignments.

Table 4-10 SYS_24MHZ Register bit assignments

Bits	Name	Function
[31:0]	24MHZ_COUNT	Contains the count, at 24MHz, from the last **CB_nRST** reset. **CB_nRST** sets the register to zero and then the count resumes.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.9 SYS_MISC Register

The SYS_MISC Register characteristics are:

Purpose
Denotes the presence or absence of a LogicTile Express daughterboard fitted in the daughterboard site.

Usage constraints
Bit[19] is read-write. Bit[13] is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

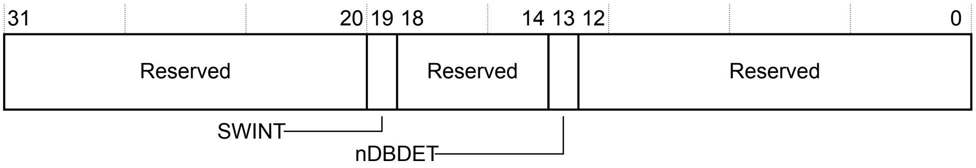


Figure 4-10 SYS_MISC Register bit assignments

The following table shows the bit assignments.

Table 4-11 SYS_MISC Register bit assignments

Bits	Name	Function
[31:20]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[19]	SWINT	Event output to daughterboard. See your daughterboard documentation for more information specific to your board.
[18:14]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[13]	nDBDET	Detect fitted daughterboard: `0b0` Daughterboard not present. `0b1` Daughterboard present.
[12:0]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.10 SYS_PCIE_CNTL Register

The SYS_PCIE_CNTL Register characteristics are:

Purpose
Error signal from PCIe switch and reset signal to PCIe Express slots.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

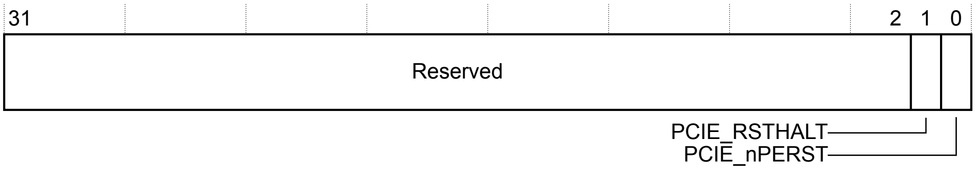


Figure 4-11 SYS_PCIE_CNTL Register bit assignments

The following table shows the bit assignments.

Table 4-12 SYS_PCIE_CNTL Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[1]	PCIE_RSTHALT	Error signal from PCIe switch.
[0]	PCIE_nPERST	Reset signal to PCIe expansion slots.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.11 SYS_PCIE_GBE Register

The SYS_PCIE_GBE Register characteristics are:

Purpose

Contains the 48-bit PCI Express Ethernet MAC address.

Usage constraints

Bits[47:0] are read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

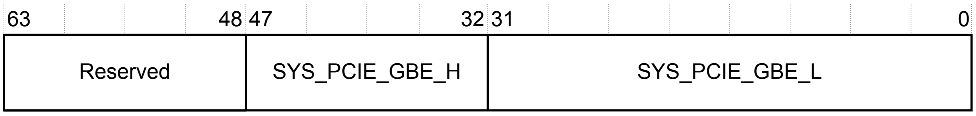


Figure 4-12 SYS_PCIE_GBE Register bit assignments

The following table shows the bit assignments.

Table 4-13 SYS_PCI_GBE Register bit assignments

Bits	Name	Function
[63:48]	-	Reserved. If you read this register, you must ignore these bits.
[47:32]	SYS_PCIE_GBE_H	Most significant 16 bits of the PCI Express Ethernet MAC address.
[31:0]	SYS_PCIE_GBE_L	Least significant 32 bits of the PCI Express Ethernet MAC address.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.12 SYS_PROC_ID0 Register

The SYS_PROC_ID0 Register characteristics are:

Purpose
Identifies the active clusters in the Juno r2 SoC.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

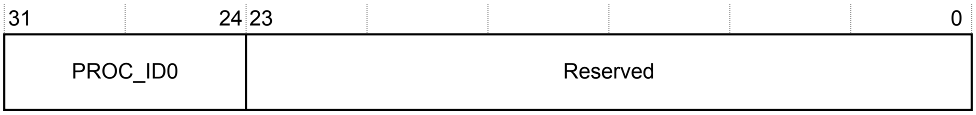


Figure 4-13 SYS_PROC_ID0 Register bit assignments

The following table shows the bit assignments.

Table 4-14 SYS_PROC_ID0 Register bit assignments

Bits	Name	Function
[31:24]	PROC_ID0	Denotes active clusters, Cortex-A72, Cortex-A53, and Mali-T624 GPU.
[23:0]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.13 SYS_PROC_ID1 Register

The SYS_PROC_ID1 Register characteristics are:

Purpose
Contains identification information about the FPGA image and the LogicTile Express daughterboard fitted to the V2M-Juno r2 motherboard.

Usage constraints
There are no usage constraints.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

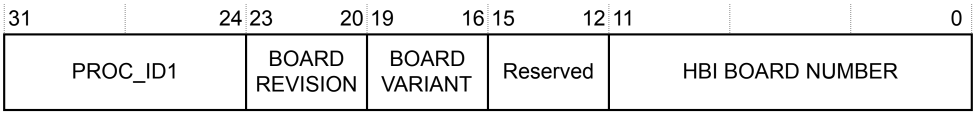


Figure 4-14 SYS_PROC_ID1 Register bit assignments

The following table shows the bit assignments.

Table 4-15 SYS_PROC_ID1 Register bit assignments

Bits	Name	Function
[31:24]	PROC_ID1	Denotes Application note or FPGA image in LogicTile daughterboard.
[23:20]	BOARD REVISION	Denotes the daughterboard revision: `0x0` A. `0x1` B. `0x2` C.
[19:16]	BOARD VARIANT	Denotes the daughterboard variant: `0x0` A. `0x1` B. `0x2` C.
[15:12]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[11:0]	HBI BOARD NUMBER	Denotes the HBI board number of the LogicTile Express daughterboard: `0x192` HBI0192. `0x217` HBI0217. `0x247` HBI0247.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.14 SYS_FAN_SPEED Register

The SYS_FAN_SPEED Register characteristics are:

Purpose

Contains a value that represents the fan operating speed. The MCC uses this value to moderate the speed of the cooling fan on the V2M-Juno r2 motherboard.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

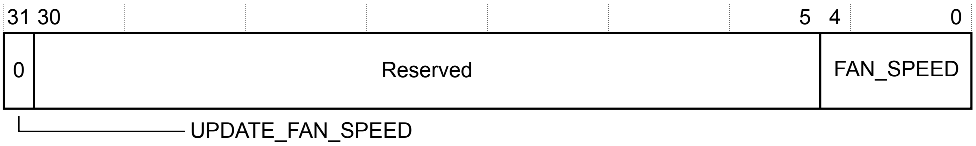


Figure 4-15 SYS_FAN_SPEED Register bit assignments

The following table shows the bit assignments.

Table 4-16 SYS_FAN_SPEED Register bit assignments

Bits	Name	Function
[31]	UPDATE_FAN_SPEED	Set this bit to `0b1` when updating the fan speed control bits [4:0]. The system clears this bit to `0b0` after updating the fan speed. The default value is `0b0`.
[30:5]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[4:0]	FAN_SPEED	Indicates and controls the speed of the board cooling fan. The fan has 30 speed settings: `0b00010` Minimum fan speed. `0b11111` Maximum fan speed. **Note** `0b00000` and `0b00001` are invalid settings. Do not use them.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.3.15 SP810_CTRL Register

The SP810_CTRL Register characteristics are:

Purpose

This register in the SP810 system controller selects the source clocks for the four SP804 timers in the IOFPGA.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

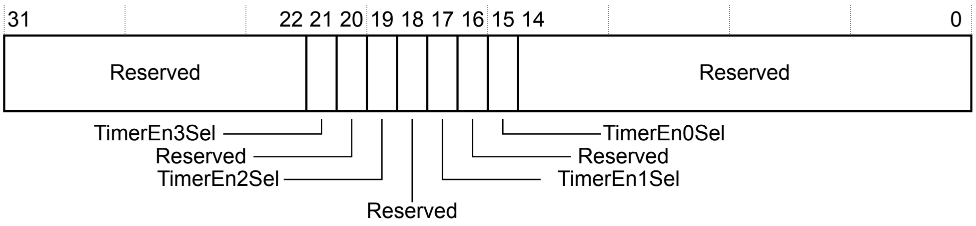


Figure 4-16 SP810_CTRL Register bit assignments

The following table shows the bit assignments.

Table 4-17 SP810_CTRL Register bit assignments

Bits	Name	Function
[31:22]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[21]	TimerEn3Sel	Selects the source clock for SP804 3 timer clock **TIM_CLK[3]**: `0b0` **TIM_CLK[3] = 32kHz**. `0b1` **TIM_CLK[3] = 1MHz**. **Note** The default is `0b0`.
[20]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[19]	TimerEn2Sel	Selects the source clock for SP804 2 timer clock **TIM_CLK[2]**: `0b0` **TIM_CLK[2] = 32kHz**. `0b1` **TIM_CLK[2] = 1MHz**. **Note** The default is `0b0`.
[18]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.
[17]	TimerEn1Sel	Selects the source clock for SP804 1 timer clock **TIM_CLK[1]**: `0b0` **TIM_CLK[1] = 32kHz**. `0b1` **TIM_CLK[1] = 1MHz**. **Note** The default is `0b0`.
[16]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.

Table 4-17 SP810_CTRL Register bit assignments (continued)

Bits	Name	Function
[15]	TimerEn0Sel	Selects the source clock for SP804 0 timer clock **TIM_CLK[0]**: `0b0` **TIM_CLK[0]** = **32kHz**. `0b1` **TIM_CLK[0]** = **1MHz**. **Note** The default is `0b0`.
[14:0]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.

Related concepts

4.3.1 APB system register summary on page 4-88.

4.4 APB system configuration registers

The IOFPGA contains the APB system configuration registers.

This section contains the following subsections:
- *4.4.1 APB system configuration register summary* on page 4-102.
- *4.4.2 SYS_CFGDATA Register* on page 4-102.
- *4.4.3 SYS_CFGCTRL Register* on page 4-103.
- *4.4.4 SYS_CFGSTAT Register* on page 4-104.

4.4.1 APB system configuration register summary

The base memory address of the APB system configuration registers is `0x1C010000`.

The following table shows the registers in address offset order from the base memory address.

Table 4-18 V2M-Juno r2 motherboard APB system configuration register summary

Offset	Name	Type	Reset	Width	Description
`0x00A0`	SYS_CFGDATA	RW	`0x00000000`	32	See *4.4.2 SYS_CFGDATA Register* on page 4-102.
`0x00A4`	SYS_CFGCTRL	RW	`0x00000000`	32	See *4.4.3 SYS_CFGCTRL Register* on page 4-103.
`0x00A8`	SYS_CFGSTAT	RW	`0x00000000`	32	See *4.4.4 SYS_CFGSTAT Register* on page 4-104.

4.4.2 SYS_CFGDATA Register

The SYS_CFGDATA_OUT Register characteristics are:

Purpose

The application software in the Juno r2 SoC writes data to the SYS_CFGDATA Register during a write operation. This data represents a value or function that the write operation sends to the addressed component, for example the frequency value of a clock generator.

The MCC or Daughterboard Configuration Controller writes return data to the SYS_CFGDATA Register during a read operation. This data represents a value or function that the read operation receives from the addressed component, for example the frequency value of a clock generator.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

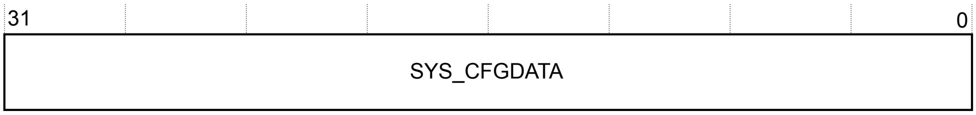


Figure 4-17 SYS_CFGDATA_OUT Register bit assignments

The following table shows the bit assignments.

Table 4-19 SYS_CFGDATA_OUT Register bit assignments

Bits	Name	Function
[31:0]	SYS_CFGDATA	Write-data or read-data.

Related concepts

4.4.1 APB system configuration register summary on page 4-102.

4.4.3 SYS_CFGCTRL Register

The SYS_CFGCTRL Register characteristics are:

Purpose

Controls write and read data transfer between the MCC and the SCC interface in the FPGA.

Usage constraints

There are no usage constraints.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

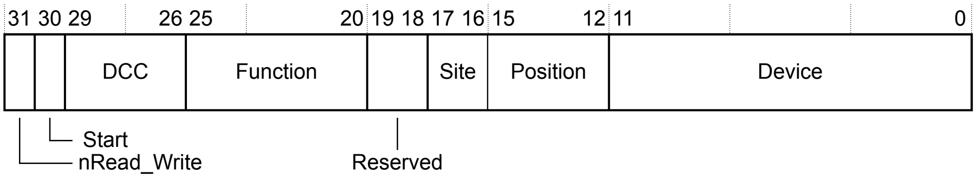


Figure 4-18 SYS_CFGCTRL Register bit assignments

The following table shows the bit assignments.

Table 4-20 SYSCFG_CTRL Register bit assignments

Bits	Name	Function
[31]	Start	Writing to this bit generates an interrupt.
[30]	nRead_Write	`0b0` Read access. `0b1` Write access.
[29:26]	DCC	4-bit number that selects the Daughterboard Configuration Controller on the daughterboard. For example: `0x0` Selects DCC 0. `0x1` Selects DCC 1.
[25:20]	Function	6-bit value that defines the function of the daughterboard device that the transaction writes to or reads from. These bits support the following functions: `0b000001` Clock generator. `0b000100` Temperature. `0b000101` Daughterboard reset register. `0b000110` SCC configuration register. `0b001000` Shut down system. `0b001001` Reboot system.
[19:18]	-	Reserved. If you write to this register, you must write all zeros to these bits. If you read this register, you must ignore these bits.

Table 4-20 SYSCFG_CTRL Register bit assignments (continued)

Bits	Name	Function
[17:16]	Site	Selects the board site location of the device to write to or read from. The V2M-Juno r2 motherboard supports the following locations: `0b00` V2M-Juno r2 motherboard. `0b01` LogicTile Express daughterboard site.
[15:12]	Position	Selects the position of the daughterboard in the stack. For example: `0x1` Daughterboard at the lowest position in the stack next to the V2M-Juno r2 motherboard. `0x2` Daughterboard 2 in the stack.
[11:0]	Device	12-bit number that denotes the device number. For example: `0x000` Selects device 0. `0x001` Selects device 1.

Related concepts

4.4.1 APB system configuration register summary on page 4-102.

4.4.4 SYS_CFGSTAT Register

The SYS_CFGSTAT Register characteristics are:

Purpose

Contains system configuration status information about read and write operations between the application software in the Juno r2 SoC and a component on a fitted LogicTile Express daughterboard or the V2M-Juno r2 motherboard.

Usage constraints

The SYS_CFGSTAT Register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

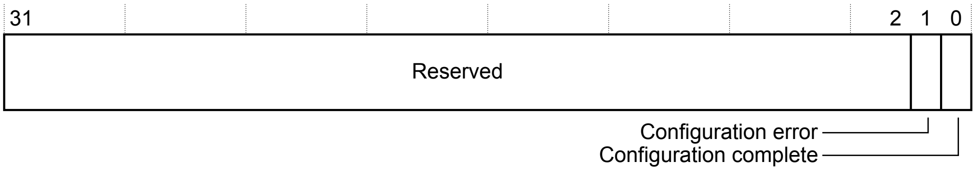


Figure 4-19 SYS_CFGSTAT Register bit assignments

The following table shows the bit assignments.

Table 4-21 SYS_CFGSTAT Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. If you read this register, you must ignore these bits.
[1]	Configuration error	A write to SYS_CFGCTRL clears this bit: `0b0` Configuration successful. `0b1` Configuration failed.
[0]	Configuration complete	A write to SYS_CFGCTRL clears this bit: `0b0` Configuration not complete. `0b1` Configuration complete.

Related concepts

4.4.1 APB system configuration register summary on page 4-102.

4.5 APB energy meter registers

The IOFPGA contains the APB energy meter registers.

This section contains the following subsections:

4.5.1 APB energy register summary

The APB energy meter registers contain values that represent supply currents, supply voltages, and power consumption in the Juno r2 SoC.

The IOFPGA provides energy registers that measure the instantaneous current consumption, instantaneous voltage supplies, instantaneous power consumption, and cumulative energy consumption of the Cortex-A72 cluster, the Cortex-A53 cluster, the Mali-T624 GPU cluster, and the fabric of the Juno r2 SoC outside the clusters, that is, the parts of the chip that operate from the VSYS power supply.

Caution

You cannot use a core in one cluster to obtain a current or power consumption value of the same cluster. Because the process of reading a current or power register alters the current and power consumption of that cluster, such a measurement is not valid.

For this reason, you cannot use a Cortex-A72 core to obtain the instantaneous current or power consumption of the Cortex-A72 cluster. You must use one of the Cortex-A53 cores to obtain these values for the Cortex-A72 cluster.

Similarly, you cannot use a Cortex-A53 core to obtain the instantaneous current or power consumption of the Cortex-A53 cluster. You must use one of the Cortex-A72 cores to obtain these values for the Cortex-A53 cluster.

Note

Providing that the measurement process takes a short time relative to the application process, you can use a core in one cluster to obtain the cumulative energy consumption of the same cluster. This is because the cumulative energy value is a long-term measurement and the short time spent in reading the energy register does not greatly affect the result.

Therefore you can use a Cortex-A72 core to measure the cumulative energy consumption of the Cortex-A72 cluster and a Cortex-A53 core to read the cumulative energy consumption of the Cortex-A53 cluster.

The following table shows the energy registers in offset order from the APB registers base memory address of `0x1C010000`.

Table 4-22 V2M-Juno r2 motherboard energy register summary

Offset	Name	Type	Reset	Width	Description
`0x00D0`	SYS_I_SYS	RO	`0x00000000`	32	See *4.5.2 SYS_I_SYS Register* on page 4-108.
`0x00D4`	SYS_I_A72	RO	`0x00000000`	32	See *4.5.3 SYS_I_A72 Register* on page 4-108.
`0x00D8`	SYS_I_A53	RO	`0x00000000`	32	See *4.5.4 SYS_I_A53 Register* on page 4-109.
`0x00DC`	SYS_I_GPU	RO	`0x00000000`	32	See *4.5.5 SYS_I_GPU Register* on page 4-109.
`0x00E0`	SYS_V_SYS	RO	`0x00000000`	32	See *4.5.6 SYS_V_SYS Register* on page 4-110.
`0x00E4`	SYS_V_A72	RO	`0x00000000`	32	See *4.5.7 SYS_V_A72 Register* on page 4-111.
`0x00E8`	SYS_V_A53	RO	`0x00000000`	32	See *4.5.8 SYS_V_A53 Register* on page 4-111.
`0x00EC`	SYS_V_GPU	RO	`0x00000000`	32	See *4.5.9 SYS_V_GPU Register* on page 4-112.
`0x00F0`	SYS_POW_SYS	RO	`0x00000000`	32	See *4.5.10 SYS_POW_SYS Register* on page 4-112.
`0x00F4`	SYS_POW_A72	RO	`0x00000000`	32	See *4.5.11 SYS_POW_A72 Register* on page 4-113.
`0x00F8`	SYS_POW_A53	RO	`0x00000000`	32	See *4.5.12 SYS_POW_A53 Register* on page 4-114.
`0x00FC`	SYS_POW_GPU	RO	`0x00000000`	32	See *4.5.13 SYS_POW_GPU Register* on page 4-114.
`0x0100`	SYS_ENM_L_SYS	RW	`0x00000000`	32	See *4.5.14 SYS_ENM_SYS Register* on page 4-115.
`0x0104`	SYS_ENM_H_SYS	RW	`0x00000000`	32	See *4.5.14 SYS_ENM_SYS Register* on page 4-115.
`0x0108`	SYS_ENM_L_A72	RW	`0x00000000`	32	See *4.5.15 SYS_ENM_A72 Register* on page 4-116.
`0x010C`	SYS_ENM_H_A72	RW	`0x00000000`	32	See *4.5.15 SYS_ENM_A72 Register* on page 4-116.
`0x0110`	SYS_ENM_L_A53	RW	`0x00000000`	32	See *4.5.16 SYS_ENM_A53 Register* on page 4-117.
`0x0114`	SYS_ENM_H_A53	RW	`0x00000000`	32	See *4.5.16 SYS_ENM_A53 Register* on page 4-117.
`0x0118`	SYS_ENM_L_GPU	RW	`0x00000000`	32	See *4.5.17 SYS_ENM_GPU Register* on page 4-118.
`0x011C`	SYS_ENM_H_GPU	RW	`0x00000000`	32	See *4.5.17 SYS_ENM_GPU Register* on page 4-118.

Related concepts

2.4.1 Power control and Dynamic Voltage and Frequency Scaling (DVFS) on page 2-26.

4.5.2 SYS_I_SYS Register

The SYS_I_SYS Register characteristics are:

Purpose
Contains a 12-bit representation of the instantaneous current consumption of the Juno r2 SoC outside the clusters.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

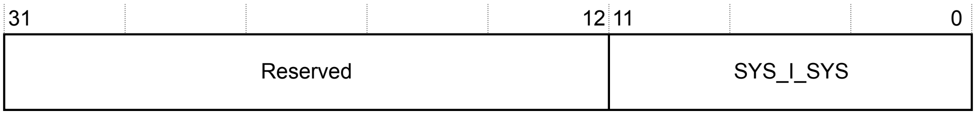


Figure 4-20 SYS_I_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-23 SYS_I_SYS Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_I_SYS	12-bit representation of the instantaneous current consumption of the Juno r2 SoC outside the clusters: • Full scale measurement, 4096, represents 5A. Full scale is `0xFFF`. • Measured current = (SYS_I_SYS+1)/761 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.3 SYS_I_A72 Register

The SYS_I_A72 Register characteristics are:

Purpose
Contains a 12-bit representation of the instantaneous current consumption of the Cortex-A72 cluster.

Usage constraints
This register is read-only. You must use one of the Cortex-A53 cores to read this register.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

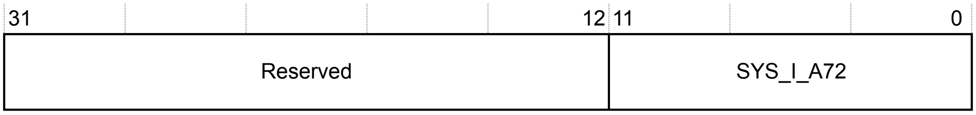


Figure 4-21 SYS_I_A72 Register bit assignments

The following table shows the bit assignments.

Table 4-24 SYS_I_A72 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_I_A72	12-bit representation of the instantaneous current consumption of the Cortex-A72 cluster: • Full scale measurement, 4096, represents 10A. Full scale is `0xFFF`. • Measured current = (SYS_I_A72+1)/381 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.4 SYS_I_A53 Register

The SYS_I_A53 Register characteristics are:

Purpose
Contains a 12-bit representation of the instantaneous current consumption of the Cortex-A53 cluster.

Usage constraints
This register is read-only. You must use one of the Cortex-A72 cores to read this register.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

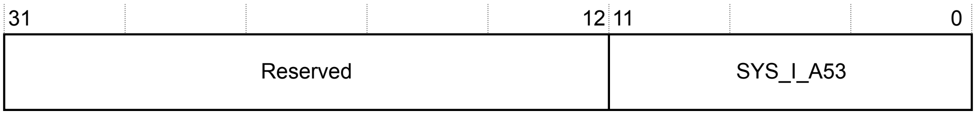


Figure 4-22 SYS_I_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-25 SYS_I_A53 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_I_A53	12-bit representation of the instantaneous current consumption of the Cortex-A53 cluster: • Full scale measurement, 4096, represents 5A. Full scale is `0xFFF`. • Measured current = (SYS_I_A53+1)/761 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.5 SYS_I_GPU Register

The SYS_I_GPU Register characteristics are:

Purpose
Contains a 12-bit representation of the instantaneous current consumption of the Mali-T624 GPU cluster.

Usage constraints
This register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

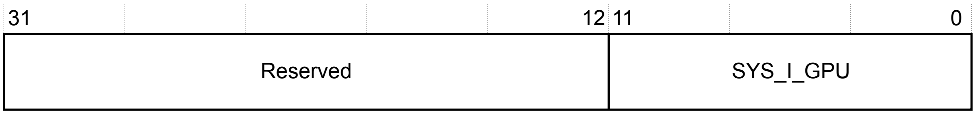


Figure 4-23 SYS_I_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-26 SYS_I_GPU Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_I_GPU	12-bit representation of the instantaneous current consumption of the Mali-T624 GPU cluster: • Full scale measurement, 4096, represents 10A. Full scale is `0xFFF`. • Measured current = (SYS_I_GPU+1)/381 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.6 SYS_V_SYS Register

The SYS_V_SYS Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of the Juno r2 SoC outside the clusters.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

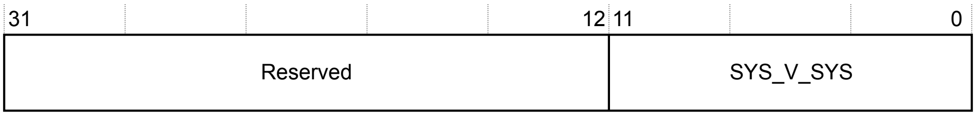


Figure 4-24 SYS_V_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-27 SYS_V_SYS Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_V_SYS	12-bit representation of the instantaneous supply voltage of the Juno r2 SoC outside the clusters: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_SYS+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.7 SYS_V_A72 Register

The SYS_V_A72 Register characteristics are:

Purpose
Contains a 12-bit representation of the instantaneous supply voltage of the Cortex-A72 cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

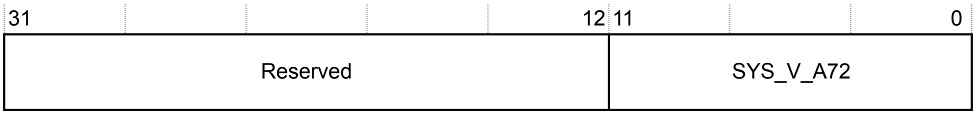


Figure 4-25 SYS_V_A72 Register bit assignments

The following table shows the bit assignments.

Table 4-28 SYS_V_A72 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_V_A72	12-bit representation of the instantaneous supply voltage of the Cortex-A72 cluster: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_A72+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.8 SYS_V_A53 Register

The SYS_V_A53 Register characteristics are:

Purpose
Contains a 12-bit representation of the instantaneous supply voltage of the Cortex-A53 cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

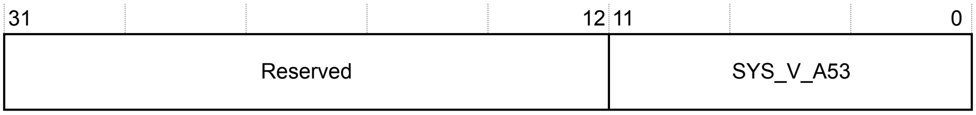


Figure 4-26 SYS_V_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-29 SYS_V_A53 Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_V_A53	12-bit representation of the instantaneous supply voltage of the Cortex-A53 cluster: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_A53+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.9 SYS_V_GPU Register

The SYS_V_GPU Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of the Mali-T624 GPU cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

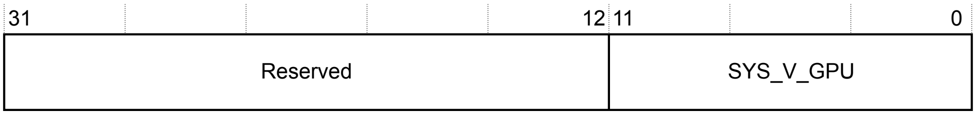


Figure 4-27 SYS_V_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-30 SYS_V_GPU Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. If you read this register, you must ignore these bits.
[11:0]	SYS_V_GPU	12-bit representation of the instantaneous supply voltage of the Mali-T624 GPU cluster: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_GPU+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.10 SYS_POW_SYS Register

The SYS_POW_SYS Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of the Juno r2 SoC outside the clusters.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

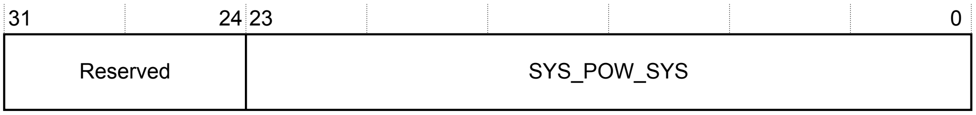


Figure 4-28 SYS_POW_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-31 SYS_POW_SYS Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. If you read this register, you must ignore these bits.
[23:0]	SYS_POW_SYS	24-bit representation of the instantaneous power consumption of the Juno r2 SoC outside the clusters: • The value of these bits represents [SYS_I_SYS(I) × SYS_V_SYS(V)]/1234803 watts. • Measured power consumption=[SYS_POW_SYS]/1234803 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.11 SYS_POW_A72 Register

The SYS_POW_A72 Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of the Cortex-A72 cluster.

Usage constraints

This register is read-only. You must use one of the cores in the Cortex-A53 cluster to read this register.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

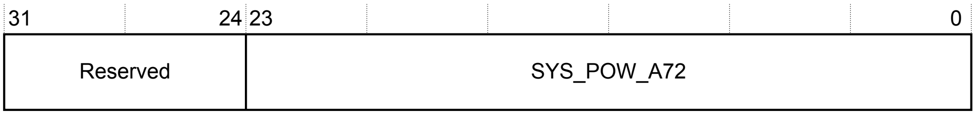


Figure 4-29 SYS_POW_A72 Register bit assignments

The following table shows the bit assignments.

Table 4-32 SYS_POW_A72 Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. If you read this register, you must ignore these bits.
[23:0]	SYS_POW_A72	24-bit representation of the instantaneous power consumption of the Cortex-A72 cluster: • The value of these bits represents [SYS_I_A72(I) × SYS_V_A72(V)]/617402 watts. • Measured power consumption=[SYS_POW_A72]/617402 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.12 SYS_POW_A53 Register

The SYS_POW_A53 Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of the Cortex-A53 cluster.

Usage constraints

This register is read-only. You must use one of the cores in the Cortex-A72 cluster to read this register.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

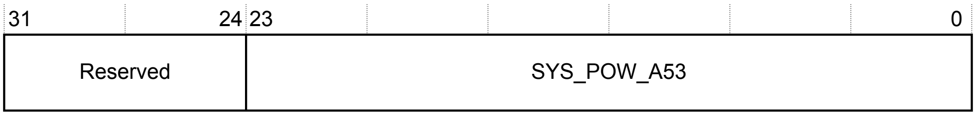


Figure 4-30 SYS_POW_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-33 SYS_POW_A53 Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. If you read this register, you must ignore these bits.
[23:0]	SYS_POW_A53	24-bit representation of the instantaneous power consumption of the Cortex-A53 cluster: • The value of these bits represents [SYS_I_A53(I) × SYS_V_A53(V)]/1234803 watts. • Measured power consumption=[SYS_POW_A53]/1234803 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.13 SYS_POW_GPU Register

The SYS_POW_GPU Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of the Mali-T624 GPU cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

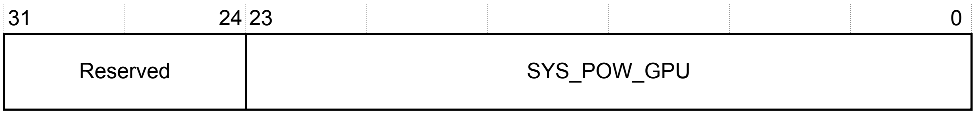


Figure 4-31 SYS_POW_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-34 SYS_POW_GPU Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. If you read this register, you must ignore these bits.
[23:0]	SYS_POW_GPU	24-bit representation of the instantaneous power consumption of the Mali-T624 GPU cluster: • The value of these bits represents [SYS_I_GPU(I) × SYS_V_GPU(V)]/617402 watts. • Measured power consumption=[SYS_POW_GPU]/617402 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.14 SYS_ENM_SYS Register

The SYS_ENM_SYS Register characteristics are:

Purpose
Contains a 64-bit representation of the accumulated energy consumption of the fabric of the Juno r2 SoC outside the clusters.

Usage constraints
Writing to this register clears the 64-bit value.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

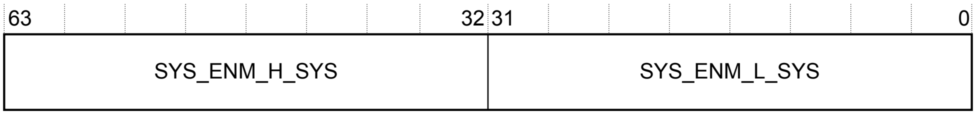


Figure 4-32 SYS_ENM_SYS Register bit assignments

The following table shows the bit assignments.

Table 4-35 SYS_ENM_SYS Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_H_SYS	Most significant 32 bits of a 64-bit representation of the accumulated energy energy consumption of the fabric of the Juno r2 SoC outside the clusters: • The memory address offset of these bits is `0x0104`. • Accumulated energy = (SYS_ENM_CH0_H_SYS:SYS_ENM_L_SYS)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_SYS	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the fabric of the Juno r2 SoC outside the clusters: • The memory address offset of these bits is `0x0100`. • Accumulated energy = (SYS_ENM_CH0_H_SYS:SYS_ENM_L_SYS)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.15 SYS_ENM_A72 Register

The SYS_ENM_A72 Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of the Cortex-A72 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

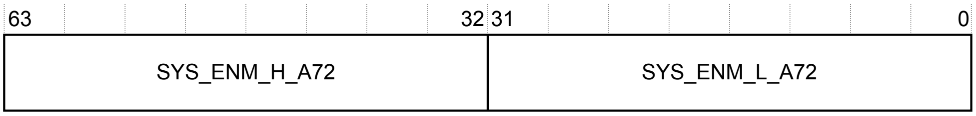


Figure 4-33 SYS_ENM_A72 Register bit assignments

The following table shows the bit assignments.

Table 4-36 SYS_ENM_A72 Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_H_A72	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Cortex-A72 cluster: • The memory address offset of these bits is `0x010C`. • Accumulated energy = (SYS_ENM_H_A72:SYS_ENM_L_A72)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_A72	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Cortex-A72 cluster: • The memory address offset of these bits is `0x0108`. • Accumulated energy = (SYS_ENM_H_A72:SYS_ENM_L_A72)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.16 SYS_ENM_A53 Register

The SYS_ENM_A53 Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of the Cortex-A53 cluster.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

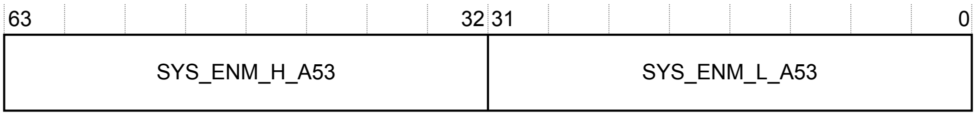


Figure 4-34 SYS_ENM_A53 Register bit assignments

The following table shows the bit assignments.

Table 4-37 SYS_ENM_A53 Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_H_A53	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Cortex-A53 cluster: • The memory address offset of these bits is `0x0114`. • Accumulated energy = (SYS_ENM_H_A53:SYS_ENM_L_A53)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_A53	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Cortex-A53 cluster: • The memory address offset of these bits is `0x0110`. • Accumulated energy = (SYS_ENM_H_A53:SYS_ENM_L_A53)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

4.5.17 SYS_ENM_GPU Register

The SYS_ENM_GPU Register characteristics are:

Purpose
Contains a 64-bit representation of the accumulated energy consumption of the Mali-T624 GPU cluster.

Usage constraints
This register is read-only.

Configurations
Available in all V2M-Juno r2 motherboard configurations.

The following figure shows the bit assignments.

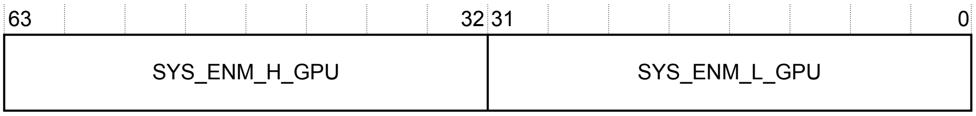


Figure 4-35 SYS_ENM_GPU Register bit assignments

The following table shows the bit assignments.

Table 4-38 SYS_ENM_GPU Register bit assignments

Bits	Name	Function
[63:32]	SYS_ENM_H_GPU	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Mali-T624 GPU cluster: • The memory address offset of these bits is `0x011C`. • Accumulated energy = (SYS_ENM_H_GPU:SYS_ENM_L_GPU)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_GPU	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the Mali-T624 GPU cluster: • The memory address offset of these bits is `0x0118`. • Accumulated energy = (SYS_ENM_H_GPU:SYS_ENM_L_GPU)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

Related concepts

4.5.1 APB energy register summary on page 4-106.

Appendix A
Signal Descriptions

This appendix describes the signals present at the interface connectors of the Versatile Express V2M-Juno r2 motherboard.

It contains the following sections:

A.1 Debug connectors

The V2M-Juno r2 motherboard provides one P-JTAG and two trace connectors for debug.

This section contains the following subsections:
- *A.1.1 P-JTAG connector* on page Appx-A-121.
- *A.1.2 Trace connectors* on page Appx-A-122.

A.1.1 P-JTAG connector

The V2M-Juno r2 motherboard provides one P-JTAG connector.

The P-JTAG connector also supports *Serial Wire Debug* (SWD).

The V2M-Juno r2 motherboard labels the P-JTAG connector as *CS_JTAG*.

The following figure shows the P-JTAG connector, J25.

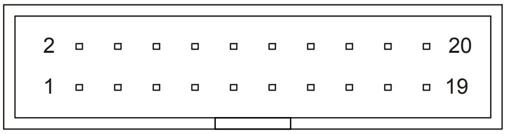


Figure A-1 P-JTAG connector, J25

The following table shows the pin mapping for the P-JTAG signals on the P-JTAG connector, J25.

Table A-1 P-JTAG connector, J25, signal list

Pin	Signal	Pin	Signal
1	**VTREFC (1V8)**	2	**CS_BS_VSUPPLY (1V8)**
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**SWDIO/TMS**	8	**GND**
9	**SWDCLK/TCK**	10	**GND**
11	**GND/RTCK**	12	**GND**
13	**SWO/TDO**	14	**GND**
15	**nSRST**	16	**GND**
17	No connection/**EDBGRQ**	18	**GNDDETECT**
19	No connection/**DBGACK**	20	**GND**

Note

- Pins 9 and 17 have pulldown resistors to 0V.
- Pin 11 has a pulldown resistor to 0V. V2M-Juno r2 motherboard does not support adaptive clocking.
- Pins 3, 5, 7, 13, 15, and 19 have pullup resistors to 1V8.
- Pins 7 and 9 are dual-mode pins that enable the Juno r2 SoC to support both the JTAG and SWD protocols.

Related concepts

2.17 Debug and trace on page 2-59.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.1.2 Trace connectors

The V2M-Juno r2 motherboard provides two debug connectors that together support 32-bit trace.

The Juno r2 SoC supports up to 32-bit trace output from the CoreSight *Trace Port Interface Unit* (TPIU) and enables connection of a compatible trace unit. Two MICTOR trace connectors, labeled *TRACEA-SINGLE* and *TraceB DUAL*, connect to the TPIU.

The two connectors support 32-bit trace when you use them together. The *TRACEA-SINGLE* connector, when you use it alone, supports 16-bit trace.

The connectors also support *Serial Wire Debug* (SWD).

Note

- *DSTREAM* is an example of a trace module that you can use.
- All trace and SWD signals operate at 1.8V.
- The trace connectors cannot supply power to a trace unit.

The following figure shows the MICTOR 38 connector.

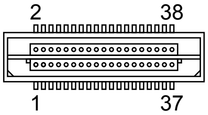


Figure A-2 MICTOR 38 connector, J27 and J28

The following table shows the pin mapping for the Trace and SWD signals on the *TRACEA-SINGLE* connector, J28.

Table A-2 TRACEA-SINGLE connector, J28, signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	No connection	4	No connection
5	**GND**	6	**TRACE_CLKA**
7	**EDBGRQ**	8	**DBGACK**
9	No connection/**nSRST**	10	**GND**
11	**TDO/SWO**	12	**1V8** reference
13	**RTCK**	14	**1V8_OUT**
15	**TCK/SWCLK**	16	**TRACEDATA[7]**
17	**TMS/SWDIO**	18	**TRACEDATA[6]**
19	**TDI**	20	**TRACEDATA[5]**
21	**nTRST**	22	**TRACEDATA[4]**
23	**TRACEDATA[15]**	24	**TRACEDATA[3]**
25	**TRACEDATA[14]**	26	**TRACEDATA[2]**
27	**TRACEDATA[13]**	28	**TRACEDATA[1]**

Table A-2 TRACEA-SINGLE connector, J28, signal list (continued)

Pin	Signal	Pin	Signal
29	**TRACEDATA[12]**	30	**GND**
31	**TRACEDATA[11]**	32	**GNDDETECT**
33	**TRACEDATA[10]**	34	**1V8** reference
35	**TRACEDATA[9]**	36	**TRACECTL**
37	**TRACEDATA[8]**	38	**TRACEDATA[0]**

Note

- The trace connector cannot supply power to a trace unit.
- The interface does not support the **TRACECTL** signal. The Juno r2 SoC always drives this signal LOW.

The following table shows the pin mapping for the trace signals on the *TraceB DUAL* connector, J27.

Table A-3 TraceB DUAL connector, J27, signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	No connection	4	No connection
5	**GND**	6	**TRACE_CLKB**
7	No connection	8	No connection
9	No connection	10	No connection
11	No connection	12	**1V8** reference
13	No connection	14	No connection
15	No connection	16	**TRACEDATA[23]**
17	No connection	18	**TRACEDATA[22]**
19	No connection	20	**TRACEDATA[21]**
21	No connection	22	**TRACEDATA[20]**
23	**TRACEDATA[31]**	24	**TRACEDATA[19]**
25	**TRACEDATA[30]**	26	**TRACEDATA[18]**
27	**TRACEDATA[29]**	28	**TRACEDATA[17]**
29	**TRACEDATA[28]**	30	**GND**
31	**TRACEDATA[27]**	32	**GND**
33	**TRACEDATA[26]**	34	**1V8** reference
35	**TRACEDATA[25]**	36	No connection
37	**TRACEDATA[24]**	38	**TRACEDATA[16]**

Related concepts

2.17 Debug and trace on page 2-59.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.2 Configuration 10Mbps Ethernet and dual-USB connector

The V2M-Juno r2 motherboard provides one connector that supports 10Mbps Ethernet access to the microSD card and provides two of the four general-purpose dual-USB 2.0 ports on the board.

The configuration 10Mbps Ethernet connects to the Ethernet LAN controller in the MCC. You can use the configuration 10Mbps Ethernet port to perform *Drag-and-Drop* configuration file editing in the V2M-Juno r2 motherboard microSD card.

The two USB 2.0 ports connect to the USB 4-port hub. They provide two of the four general-purpose USB 2.0 ports on the V2M-Juno r2 motherboard.

The following figure shows the configuration 10Mbps Ethernet and dual-USB 2.0 connector, J40.

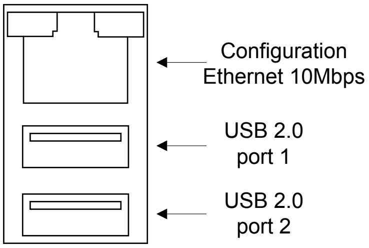


Figure A-3 Configuration 10Mbps Ethernet and dual-USB 2.0 connector, J40

Related concepts

2.11 USB 2.0 interface on page 2-50.

3.3.1 Overview of configuration files and microSD card directory structure on page 3-70.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.3 PCI Express Gigabit Ethernet and dual-USB connector

The V2M-Juno r2 motherboard provides a combined Gigabit Ethernet and dual-USB connector that supports Ethernet access to the PCIe switch and provides two of the four general-purpose USB 2.0 ports on the board.

The Gigabit Ethernet port connects to the Gigabit Ethernet controller that provides access to the PCIe switch on the V2M-Juno r2 motherboard.

The two USB 2.0 ports connect to the USB 4-port hub. They provide two of the four general-purpose USB 2.0 ports on the V2M-Juno r2 motherboard.

The following figure shows the PCIe Gigabit Ethernet and dual-USB 2.0 connector, J37.

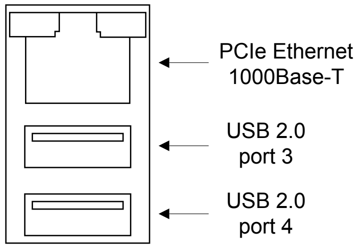


Figure A-4 PCIe Gigabit Ethernet and dual-USB 2.0 connector, J37

Related concepts

2.11 USB 2.0 interface on page 2-50.

2.14.4 Gigabit Ethernet port on page 2-55.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.4 SMC 10/100 Ethernet connector

The V2M-Juno r2 motherboard provides one SMC 10/100 Ethernet connector.

The following figure shows the SMC 10/100 Ethernet connector, J50.

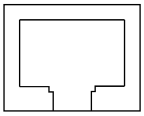


Figure A-5 SMC 10/100 Ethernet connector, J50

Related concepts

2.12 SMC 10/100 Ethernet interface on page 2-51.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.5 Configuration USB connector

The configuration USB connector provides access to the root directory and subdirectories of the microSD card.

You can use the configuration USB port to perform *Drag-and-Drop* configuration file editing in the V2M-Juno r2 motherboard configuration microSD card.

The following figure shows the configuration USB 2.0 connector, J48.

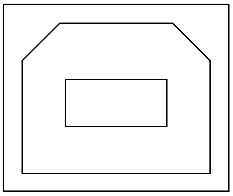


Figure A-6 Configuration USB 2.0 connector, J48

Related concepts

3.3.1 Overview of configuration files and microSD card directory structure on page 3-70.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.6 Header connectors

Two high-density header connectors enable you to fit a LogicTile FPGA board to the daughterboard site on the V2M-Juno r2 motherboard.

Header X, J1, routes the Thin Links buses between the Juno r2 SoC on the V2M-Juno r2 motherboard and the FPGA on the LogicTile daughterboard fitted in the daughterboard site.

Header Y, J4, routes the buses and power interconnect between the V2M-Juno r2 motherboard and the LogicTile FPGA daughterboard.

The constraints file, *an415_wrapper.xdc*, available in *AN415 Example Express 20MG design for a V2M-Juno Motherboard*, lists the header signals.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.7 Keyboard and Mouse Interface (KMI) connector

The V2M-Juno r2 motherboard provides a dual mini-DIN connector that supports PS/2 keyboard and mouse input to the Juno r2 SoC.

The following figure shows the dual-mini-DIN KMI connector, J59.

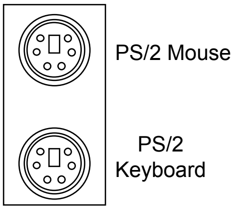


Figure A-7 Dual mini-DIN KMI connector, J59

Related concepts

2.15 Keyboard and mouse interface on page 2-56.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.8 HDMI connectors

Two female HDMI connectors provide digital video and digital audio to external displays.

The following figure shows the HDMI connectors, J53 and J54.

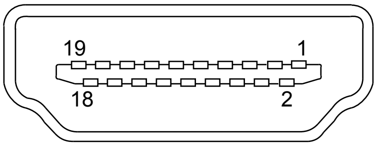


Figure A-8 HDMI connector, J53 and J54

The following table shows the pin mapping for the HDMI signals, that include encoded I^2S digital audio, on the HDMI connectors.

Table A-4 HDMI connectors, J53 and J54, signal list

Pin	Signal	Pin	Signal
1	**DVI_TX2P**	2	**GND**
3	**DVI_TX2N**	4	**DVI_TX1P**
5	**GND**	6	**DVI_TX1N**
7	**DVI_TX0P**	8	**GND**
9	**DVI_TX0N**	10	**DVI_TXCP**
11	**GND**	12	**DVI_TXCN**
13	**DVI_CECAO**	14	No connection
15	**DVI_DSCLO**	16	**DVI_DSDAO**
17	**GND**	18	**DVI_5V0**
19	**DVI_HPDO**	-	-

Related concepts

2.9 HDLCD interface on page 2-45.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.9 PCI Express expansion slots

The V2M-Juno r2 motherboard provides several PCIe slots that connect to the on-board switch.

This section contains the following subsections:

- *A.9.1 PCI Express ×4 connectors, one-lane slot 0 and slot 1* on page Appx-A-132.
- *A.9.2 PCI Express ×8 connector, four-lane slot 2* on page Appx-A-134.
- *A.9.3 PCI Express ×16 connector, four-lane slot 3* on page Appx-A-136.

A.9.1 PCI Express ×4 connectors, one-lane slot 0 and slot 1

The V2M-Juno r2 motherboard provides two PCIe ×4 connectors that each provide one lane. The board uses one lane on each connector and does not use the other six lanes.

Note

The PCIe I/O voltage at the connectors is 3.3V.

The following figure shows the PCIe ×4 connectors, one-lane slots 0 and 1, connectors J10 and J11.

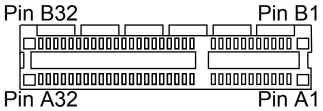


Figure A-9 PCIe ×4 connector, one-lane slots 0 and 1, connectors J10 and J11

The following table shows the pin mapping for the one-lane PCI ×4 connector, one-lane slot 0, that is, connector J11.

Table A-5 PCIe one-lane slot 0, connector J11, signal list

Pin	Signal	Pin	Signal
B1	**12V**	A1	**GND**
B2	**12V**	A2	**12V**
B3	**12V**	A3	**12V**
B4	**GND**	A4	**GND**
B5	No connection	A5	No connection
B6	No connection	A6	**PCIE_LOOP4**
B7	**GND**	A7	**PCIE_LOOP4**
B8	**3V3**	A8	No connection
B9	No connection	A9	**3V3**
B10	**3V3**	A10	**3V3**
B11	**PCIE_nWAKE0**	A11	**PCIE_nPERST5**
B12	No connection	A12	**GND**
B13	**GND**	A13	**PCIE_CLKP8**
B14	**PCIE_PETP2**	A14	**PCIE_CLKN8**
B15	**PCIE_PETN2**	A15	**GND**
B16	**GND**	A16	**PCIE_PERP2**

Table A-5 PCIe one-lane slot 0, connector J11, signal list (continued)

Pin	Signal	Pin	Signal
B17	**PCIE_nPRSNT4**	A17	**PCIE_PERN2**
B18	**GND**	A18	**GND**
B19	No connection	A19	No connection
B20	No connection	A20	**GND**
B21	**GND**	A21	No connection
B22	**GND**	A22	No connection
B23	No connection	A23	**GND**
B24	No connection	A24	**GND**
B25	**GND**	A25	No connection
B26	**GND**	A26	No connection
B27	No connection	A27	**GND**
B28	No connection	A28	**GND**
B29	**GND**	A29	No connection
B30	No connection	A30	No connection
B31	**PCIE_nPRSNT4**	A31	**GND**
B32	**GND**	A32	No connection

The following table shows the pin mapping for the one-lane PCI ×4 connector, one-lane slot 1, that is, connector J10.

Table A-6 PCIe one-lane slot 1, connector J10, signal list

Pin	Signal	Pin	Signal
B1	**12V**	A1	**GND**
B2	**12V**	A2	**12V**
B3	**12V**	A3	**12V**
B4	**GND**	A4	**GND**
B5	No connection	A5	No connection
B6	No connection	A6	**PCIE_LOOP3**
B7	**GND**	A7	**PCIE_LOOP3**
B8	**3V3**	A8	No connection
B9	No connection	A9	**3V3**
B10	**3V3**	A10	**3V3**
B11	**PCIE_nWAKE0**	A11	**PCIE_nPERST4**
B12	No connection	A12	**GND**
B13	**GND**	A13	**PCIE_CLKP7**
B14	**PCIE_PETP3**	A14	**PCIE_CLKN7**

Table A-6 PCIe one-lane slot 1, connector J10, signal list (continued)

Pin	Signal	Pin	Signal
B15	**PCIE_PETN3**	A15	**GND**
B16	**GND**	A16	**PCIE_PERP3**
B17	**PCIE_nPRSNT3**	A17	**PCIE_PERN3**
B18	**GND**	A18	**GND**
B19	No connection	A19	No connection
B20	No connection	A20	**GND**
B21	**GND**	A21	No connection
B22	**GND**	A22	No connection
B23	No connection	A23	**GND**
B24	No connection	A24	**GND**
B25	**GND**	A25	No connection
B26	**GND**	A26	No connection
B27	No connection	A27	**GND**
B28	No connection	A28	**GND**
B29	**GND**	A29	No connection
B30	No connection	A30	No connection
B31	**PCIE_nPRSNT3**	A31	**GND**
B32	**GND**	A32	No connection

Related concepts

2.14.2 PCI Express expansion slots on page 2-54.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.9.2 PCI Express ×8 connector, four-lane slot 2

The V2M-Juno r2 motherboard provides one PCIe ×8 connector that provides four PCIe lanes. The board uses four lanes of the eight, and does not use the other four lanes.

Note

The PCIe I/O voltage at the connector is 3.3V.

The following figure shows the PCIe ×8 connector, four-lane slot 2, connector J8.

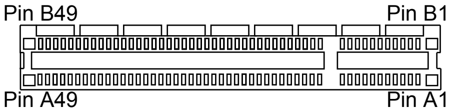


Figure A-10 PCIe ×8 connector, four-lane slot 2, connector J8

The following table shows the pin mapping for the four-lane PCIe ×8 connector, four-lane slot 2, connector J8.

Table A-7 PCIe four-lane slot 2, connector J8, signal list

Pin	Signal	Pin	Signal
B1	**12V**	A1	**GND**
B2	**12V**	A2	**12V**
B3	**12V**	A3	**12V**
B4	**GND**	A4	**GND**
B5	No connection	A5	No connection
B6	No connection	A6	**PCIE_LOOP2**
B7	**GND**	A7	**PCIE_LOOP2**
B8	**3V3**	A8	No connection
B9	No connection	A9	**3V3**
B10	**3V3**	A10	**3V3**
B11	**PCIE_nWAKE0**	A11	**PCIE_nPERST3**
B12	No connection	A12	**GND**
B13	**GND**	A13	**PCIE_CLKP6**
B14	**PCIE_PETP12**	A14	**PCIE_CLKN6**
B15	**PCIE_PETN12**	A15	**GND**
B16	**GND**	A16	**PCIE_PERP12**
B17	**PCIE_nPRSNT2**	A17	**PCIE_PERN12**
B18	**GND**	A18	**GND**
B19	**PCIE_PETP13**	A19	No connection
B20	**PCIE_PETN13**	A20	**GND**
B21	**GND**	A21	**PCIE_PERP13**
B22	**GND**	A22	**PCIE_PERN13**
B23	**PCIE_PETP14**	A23	**GND**
B24	**PCIE_PETN14**	A24	**GND**
B25	**GND**	A25	**PCIE_PERP14**
B26	**GND**	A26	**PCIE_PERN14**
B27	**PCIE_PETP15**	A27	**GND**
B28	**PCIE_PETN15**	A28	**GND**
B29	**GND**	A29	**PCIE_PERP15**
B30	No connection	A30	**PCIE_PERN15**
B31	**PCIE_nPRSNT2**	A31	**GND**
B32	**GND**	A32	No connection
B33	No connection	A33	No connection
B34	No connection	A34	**GND**
B35	**GND**	A35	No connection

Table A-7 PCIe four-lane slot 2, connector J8, signal list (continued)

Pin	Signal	Pin	Signal
B36	**GND**	A36	No connection
B37	No connection	A37	**GND**
B38	No connection	A38	**GND**
B39	**GND**	A39	No connection
B40	**GND**	A40	No connection
B41	No connection	A41	**GND**
B42	No connection	A42	**GND**
B43	**GND**	A43	No connection
B44	**GND**	A44	No connection
B45	No connection	A45	**GND**
B46	No connection	A46	**GND**
B47	**GND**	A47	No connection
B48	**PCIE_nPRSNT2**	A48	No connection
B49	**GND**	A49	**GND**

Related concepts

2.14.2 PCI Express expansion slots on page 2-54.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.9.3 PCI Express ×16 connector, four-lane slot 3

The V2M-Juno r2 motherboard provides one PCIe ×16 connector that provides four PCIe lanes. The board uses four lanes of the 16, and does not use the other 12 lanes.

Note

The PCIe IO voltage at the connector is 3.3V.

The following figure shows the PCIe ×16 connector, four-lane slot 3, connector J9.

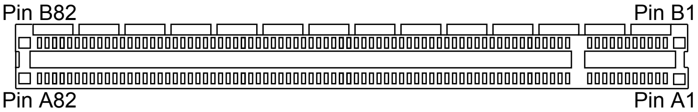


Figure A-11 PCIe ×16 connector, four-lane slot 3, connector J9

The following table shows the pin mapping for the four-lane PCIe ×16 connector, four-lane slot 3, connector J9.

Table A-8 PCIe four-lane slot 3, connector J9, signal list

Pin	Signal	Pin	Signal
B1	**12V**	A1	**GND**
B2	**12V**	A2	**12V**
B3	**12V**	A3	**12V**
B4	**GND**	A4	**GND**
B5	No connection	A5	No connection
B6	No connection	A6	**PCIE_LOOP1**
B7	**GND**	A7	**PCIE_LOOP1**
B8	**3V3**	A8	No connection
B9	No connection	A9	**3V3**
B10	**3V3**	A10	**3V3**
B11	**PCIE_nWAKE0**	A11	**PCIE_nPERST2**
B12	No connection	A12	**GND**
B13	**GND**	A13	**PCIE_CLKP5**
B14	**PCIE_PETP8**	A14	**PCIE_CLKN5**
B15	**PCIE_PETN8**	A15	**GND**
B16	**GND**	A16	**PCIE_PERP8**
B17	**PCIE_nPRSNT1**	A17	**PCIE_PERN8**
B18	**GND**	A18	**GND**
B19	**PCIE_PETP9**	A19	No connection
B20	**PCIE_PETN9**	A20	**GND**
B21	**GND**	A21	**PCIE_PERP9**
B22	**GND**	A22	**PCIE_PERN9**
B23	**PCIE_PETP10**	A23	**GND**
B24	**PCIE_PETN10**	A24	**GND**
B25	**GND**	A25	**PCIE_PERP10**
B26	**GND**	A26	**PCIE_PERN10**
B27	**PCIE_PETP11**	A27	**GND**
B28	**PCIE_PETN11**	A28	**GND**
B29	**GND**	A29	**PCIE_PERP11**
B30	No connection	A30	**PCIE_PERN11**
B31	**PCIE_nPRSNT1**	A31	**GND**
B32	**GND**	A32	No connection
B33	No connection	A33	No connection
B34	No connection	A34	**GND**
B35	**GND**	A35	No connection

Table A-8 PCIe four-lane slot 3, connector J9, signal list (continued)

Pin	Signal	Pin	Signal
B36	**GND**	A36	No connection
B37	No connection	A37	**GND**
B38	No connection	A38	**GND**
B39	**GND**	A39	No connection
B40	**GND**	A40	No connection
B41	No connection	A41	**GND**
B42	No connection	A42	**GND**
B43	**GND**	A43	No connection
B44	**GND**	A44	No connection
B45	No connection	A45	**GND**
B46	No connection	A46	**GND**
B47	**GND**	A47	No connection
B48	**PCIE_nPRSNT2**	A48	No connection
B49	**GND**	A49	**GND**
B50	No connection	A50	No connection
B51	No connection	A51	**GND**
B52	**GND**	A52	No connection
B53	**GND**	A53	No connection
B54	No connection	A54	**GND**
B55	No connection	A55	**GND**
B56	**GND**	A56	No connection
B56	**GND**	A56	No connection
B57	No connection	A57	**GND**
B58	No connection	A58	**GND**
B59	No connection	A59	**GND**
B60	**GND**	A60	No connection
B61	**GND**	A61	No connection
B62	No connection	A62	**GND**
B63	No connection	A63	**GND**
B64	**GND**	A64	No connection
B65	**GND**	A65	No connection
B66	No connection	A66	**GND**
B67	No connection	A67	**GND**
B68	**GND**	A68	No connection
B69	**GND**	A69	No connection

Table A-8 PCIe four-lane slot 3, connector J9, signal list (continued)

Pin	Signal	Pin	Signal
B70	No connection	A70	**GND**
B71	No connection	A71	**GND**
B72	**GND**	A72	No connection
B73	**GND**	A73	No connection
B74	No connection	A74	**GND**
B75	No connection	A75	**GND**
B76	**GND**	A76	No connection
B77	**GND**	A77	No connection
B78	No connection	A78	**GND**
B79	No connection	A79	**GND**
B80	**GND**	A80	No connection
B81	**PCIE_nPRSNT1**	A81	No connection
B82	No connection	A82	**GND**

Related concepts

2.14.2 PCI Express expansion slots on page 2-54.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.10 SATA 2.0 connectors

The V2M-Juno r2 motherboard provides two SATA 2.0 connectors that connect to an on-board SATA 2.0 controller with a one-lane connection to the PCIe switch.

Note

The SATA 2.0 I/O voltage at the connectors is 1.8V.

The V2M-Juno r2 motherboard labels the SATA 2.0 connectors as *SATA0* and *SATA1*. The following figure shows the SATA 2.0 connectors, SATA 0, J39 and SATA 1, J38.

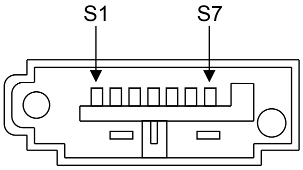


Figure A-12 SATA 2.0 connectors, J38 and J39

The following table shows the pin mapping for the SATA 0 connector, J39.

Table A-9 SATA0 connector, J39, signal list

SATA connector pin number	SATA connector pin name	Motherboard signal to SATA 2.0 controller
S1	**GND**	-
S2	**A+**	**SATA_TX0_P_C**
S3	**A-**	**SATA_TX0_N_C**
S4	**GND**	-
S5	**B-**	**SATA_RX0_N_C**
S6	**B+**	**SATA_RX0_P_C**
S7	**GND**	-

The following table shows the pin mapping for the SATA 1 connector, J38.

Table A-10 SATA1 connector, J38, signal list

SATA connector pin number	SATA connector pin name	Motherboard signal to SATA 2.0 controller
S1	**GND**	-
S2	**A+**	**SATA_TX1_P_C**
S3	**A-**	**SATA_TX1_N_C**
S4	**GND**	-
S5	**B-**	**SATA_RX1_N_C**
S6	**B+**	**SATA_RX1_P_C**
S7	**GND**	-

Related concepts

2.14.3 SATA 2.0 ports on page 2-55.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

A.11 Dual-UART connector

One dual-UART connector provides access to the MCC.

The UART port enables you to access the command-line interface in the MCC and perform application software debugging.

Note

The UART I/O voltage at the connectors is 3.3V.

The following figure shows the dual-UART connector, J57.

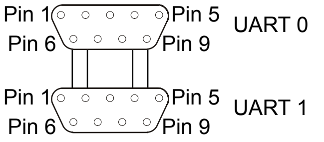


Figure A-13 Dual-UART connector, J57A, upper, and J57B, lower

The following table shows the pin mapping for UART 0. This is the upper connector, J57A, of the dual-UART connector, J57.

Table A-11 UART 0 connector, J57A, signal list

Pin	Signal
A1	No connection
A2	**SER0_RX**
A3	**SER0_TX**
A4	**SER0_DTR**
A5	**GND**
A6	**SER0_DSR**
A7	**SER0_RTS**
A8	**SER0_CTS**
A9	No connection

The following table shows the pin mapping for UART 1. This is the lower connector, J57B, of the dual-UART connector, J57.

Table A-12 UART 1 connector, J57B, signal list

Pin	Signal
A1	No connection
A2	**SER1_RX**
A3	**SER1_TX**
A4	**SER1_DTR**
A5	**GND**
A6	**SER1_DSR**
A7	**SER1_RTS**

Table A-12 UART 1 connector, J57B, signal list (continued)

Pin	Signal
A8	**SER1_CTS**
A9	No connection

Related concepts

2.13 UART interface on page 2-52.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.12 Secure keyboard and user push buttons connector

One 9-pin mini-DIN connector supports additional key entry to the V2M-Juno r2 motherboard.

The following figure shows the secure keyboard and user push buttons connector, J58.

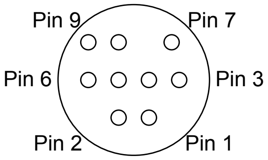


Figure A-14 Secure keyboard connector, J58

The following table shows the pin mapping for the secure keyboard and user push buttons connector, J58.

Table A-13 Secure keyboard and user push buttons connector, J58, signal list

Pin	Signal
1	**SEC_DF**
2	**SEC_PB0**
3	**GND**
4	**SEC_PB1**
5	**5V_KMI**
6	**SEC_CF**
7	**SEC_PB2**
8	**SEC_PB3**
9	**SEC_PB4**

Related concepts

2.16 Additional user key entry on page 2-57.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

1.4 Connectors on front and rear panels on page 1-16.

A.13 ATX power connector

The V2M-Juno r2 motherboard provides one power connector that enables connection of a unit that ARM supplies with the V2M-Juno r2 motherboard. This unit converts AC mains power to DC power to supply the board.

The following figure shows the ATX power connector, J20.

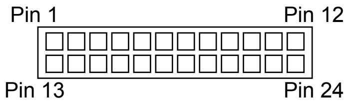


Figure A-15 ATX power connector, J20

The following table shows the pin mapping for the ATX power connector, J20, on the V2M-Juno r2 motherboard.

Table A-14 ATX power connector, J20, signal list

Pin	Signal	Pin	Signal
1	**3V3**	13	**3V3**
2	**3V3**	14	**-12V**
3	**GND**	15	**GND**
4	**5V**	16	**nATXON**
5	**GND**	17	**GND**
6	**5V**	18	**GND**
7	**GND**	19	**GND**
8	**PWOK**	20	No connection
9	**SB_5V**	21	**5V**
10	**12V**	22	**5V**
11	**12V**	23	**5V**
12	**3V3**	24	**GND**

Related concepts

2.3 External power on page 2-25.

Related references

1.3 Location of components on the V2M-Juno r2 motherboard on page 1-15.

Appendix B
Specifications

This appendix contains the electrical specifications of the Versatile Express V2M-Juno r2 motherboard.

It contains the following sections:
- *B.1 Electrical specification* on page Appx-B-147.

B.1 Electrical specification

This appendix contains electrical operating information for the Juno r2 SoC.

The following table provides the maximum operating frequencies of the Cortex-A72 cluster, Cortex-A53 cluster, and Mali-T624 GPU power domains at supply voltages of 0.8V, 0.9V, and 1.0V.

Table B-1 Cortex-A72, Cortex-A53, and Mali-T624 GPU maximum operating frequencies

Operating voltage	Cortex-A72	Cortex-A53	Mali-T624 GPU
0.8V Underdrive	600MHz	450MHz	450MHz
0.9V Nominal	1GHz	800MHz	600MHz
1.0V Overdrive	1.2GHz	950MHz	Not supported

Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following sections:
- *C.1 Revisions* on page Appx-C-149.

C.1 Revisions

The following table describes the technical changes between released issues of this book.

Table C-1 Issue 0200-00

Change	Location	Affects
No changes, first release	-	-