Application Note 53

Configuring ARM Caches

Document number: ARM DAI 0053B
Issued: February 1998
Copyright Advanced RISC Machines Ltd (ARM) 1998
# Application Note 53

## Table of Contents

1 Introduction 2

2 Overview 3
   2.1 Memory Management Unit (MMU) 3
   2.2 Protection Unit (PU) 3

3 Example 4
   3.1 Memory layout 4
   3.2 Assembler source 5
   3.3 C source 7

4 ARMulator 9
   4.1 Introduction 9
   4.2 The armul.cnf file 9
1 Introduction

In order to get maximum performance from processors such as ARM710a and StrongARM SA-110 it is necessary to enable the cache. An application may have this done for it by, for example, the underlying microkernel on the system. However, if there is no such kernel an application will have to enable the caches itself.

There are two main cache systems used on ARM processors. These are:

- Memory Management Unit (for example ARM610, ARM710a, SA-110)
- Protection Unit (for example ARM940T)

This Application Note presents some sample code for enabling the cache on both types of ARM processor, and an overview of the PageTables module from ARMulator.

It also discusses:

- repetitive assembly in armasm and tasm
- armasm and tasm conditional assembly
- macros in armasm and tasm
- inline assembler with the C compiler
- inline functions
2 Overview

2.1 Memory Management Unit (MMU)

The memory management unit provides a full virtual memory system. For a fuller description refer to the ARM Architecture Reference Manual (ARM DDI 0100).

In brief, it uses off-chip page tables to describe to the processor:

- A virtual to physical address mapping
- Access permissions
- Cache and write-buffer control.

Three sizes of page (1MB, 64kB and 4kB) are supported. (Sub-pages of 16kB and 1kB are also provided for access control.) An additional system of “Domains” operates to provide efficient access protection in a multithreaded environment.

This system allows, for example, multiple virtual address spaces with demand paging and swapping. Flavors of the UNIX operating-system have been ported to ARM-powered computers using such a memory management unit.

The advantages of this system are:

- Full control over memory at a fine granularity
- Domain-based protection
- Virtual to physical address translation.

The main disadvantage is that it requires in-memory pagetables (the cache cannot be enabled without MMU enabled).

2.2 Protection Unit (PU)

The protection unit provides access and cache control, for a more embedded environment. For a fuller description refer to the ARM940T Data Sheet (ARM DDI 0092).

In brief, the protection unit has a set of on-chip registers, which hold descriptions of:

- Access permissions
- Cache and write-buffer control

for up to eight (programmable) regions of memory.

This system allows basic memory protection and cache control for use in, for example, an embedded application.

The advantages of this system are:

- Access control held entirely on-chip (no need for any off-chip tables)
- Provides four levels of access control, cache and write-buffer control
- Separate control over instruction and data caches.

The disadvantages are:

- Small number of regions
- Restrictions on region size and alignment.
3 Example

3.1 Memory layout

Although the two systems are different, both use coprocessor 15 to control the system. Both systems have enough common functionality to distinguish which is in use. As an example, consider the memory map shown in Figure 1: Example memory layout.

![Example memory layout](image)

The shaded areas are marked not cachable and not bufferable.

- The bottom 16MB of memory are marked as cacheable. This is where application code and the heap would be based.
- One megabyte of memory immediately below 2GB is also marked as cacheable, as this is where the stack is placed.
- The rest of memory is neither cacheable nor bufferable. A real system may also mark that memory as "no access" (abort generating).

Code to set up this memory map is given in C and ARM Assembler.

The MMU architecture requires the top-level page table to be aligned to a 16kB boundary. As it is not possible to specify alignment from the C compiler, an assembler file is needed.

The sample C code makes use of the inline assembler feature of the compiler to control coprocessor 15. This code can be used in full, or stripped down for a specific processor.
3.2 Assembler source

By default, this code defines an empty pagetable, which the C code will later fill in with the pagetable entries.

The empty table uses the ALIGN and NOINIT AREA directives to ensure that the area is aligned to a 16kB \(2^{14}\) boundary and is allocated at runtime.

A different approach is to generate a fixed pagetable at compile-time using the assembler. This code is also supplied, but is not assembled.

The following section describes some of the techniques used to generate this table. For a complete description of the assembler, refer to the Software Development Toolkit Reference Guide (ARM DUI 0041).

3.2.1 Repetitive assembly

The second approach uses repetitive assembly to generate a pagetable. The following code fragment (from pagetab.s) demonstrates this idea:

```assembly
GBLA    counter
counter SETA 0
; area 1 - 0->16MB, cacheable
WHILE counter < 16
L1Entry SECTION, (counter:SHL:20), 0, \n   C_BIT+B_BIT, ALL_ACCESS
counter SETA counter + 1
WEND
```

Where:

- **GBLA counter** declares a global numeric variable called `counter` which is initialized to zero using the SETA directive.
- The **WHILE ... WEND** construct is used to assemble the lines repeatedly between **WHILE** and **WEND**.
- In this example, the loop body is assembled for `counter = 0, 1, 2 ... 14 and 15`, but because the looping condition is checked at the top of the loop, it is possible for the code between a **WHILE** and a **WEND** never to be assembled. For example, if `counter` were initialized to 16, the body of the **WHILE** ... **WEND** loop would not be assembled at all.
- Each time around the loop the macro `L1Entry` is called (with five arguments), and `counter` is incremented.
3.2.2 Macro usage and conditional assembly

The following code fragment for L1Entry is also taken from pagetab.s:

```
MACRO
    L1Entry $type, $addr, $dom, $ucb, $acc
    [ $type = SECTION
        DCD ( (($addr) :AND: &FFF0000) :OR: \ 
            (($acc) :SHL: 10) :OR: \ 
            (($dom) :SHL: 5) :OR: $ucb :OR: $type )
        MEXIT
    ]
    [ $type = PAGE
        DCD ( (($addr) :AND: &FFFFFC00) :OR: \ 
            (($dom) :SHL: 5) :OR: \ 
            (($ucb) :AND: U_BIT) :OR: $type )
        | DCD 0 ; Invalid Level 1 Page Table Entry
    ]
MEND
```

Note that a backslash breaks a logical line of assembly language across two physical lines. However, there must be no character after the backslash on the line.

The macro definition is enclosed between MACRO and MEND. The first line of the definition gives the macro’s name and lists its parameters.

The body of the macro illustrates the use of [ (IF) ... ] (ENDIF) and [ (IF) ... | (ELSE) ... ] (ENDIF) to assemble different code conditional on a value known at assembly-time. In this example, the controlling expressions of the IFS involve a macro parameter ($type) which gets its value when the macro is used.

This macro definition also uses the MEXIT directive to exit processing of a macro before the MEND directive is reached. (The MEXIT directive is similar to a return statement in a C function.)

3.2.3 The pagetab.s file

The pagetab.s file can be found at:

http://www.arm.com/Documentation/AppNotes/code/an53.zip
3.3 C source

encache.c contains code for enabling the cache and creating a page table. Since the cache is controlled via coprocessor 15, and there is no mechanism in standard C to access coprocessor registers, this code uses the __asm extension to do so. Refer to the Software Development Toolkit Reference Guide (ARM DUI 0041) for complete details of the C compiler.

The code exports a function, initMMU, which examines coprocessor 15 to determine the processor type and initialize the cache appropriately.

Since this code accesses coprocessor 15 it must be called only from a privileged mode. If called from User Mode, the accesses are ignored by the MMU or PU, and the ARM faults the instructions as undefined.

3.3.1 Inlined functions

For example, the function, from encache.c:

```c
__inline unsigned long readCP15R0(void)
{
    unsigned long id;
    __asm { MRC P15, 0, id, c0, c0; }
    return id;
}
```

uses both the __inline and __asm directives of the compiler.

__inline instructs the compiler to generate the code at point of use, rather than creating a function and calling it.

As __asm is a statement block rather than an expression, it cannot easily be made into a macro.

Later __inline functions, such as mmuFlushCache, contain conditional statements. However, these are optimized away by the compiler, as the function is called with a known argument.

Note: Inlining of functions is disabled by the compiler when the -g (generate debug tables) command line option is given.

3.3.2 The inline assembler

__asm introduces an assembler statement block. This is used as there is no other way for the compiler to generate an MCR (read coprocessor) instruction. The compiler is left to allocate a register for id and generate an appropriate instruction for it. This demonstrates one use of __asm.

Other __asm statements, such as in puWriteRegion0, use more complicated expressions as arguments in the inline assembler. The compiler generates the code for this expression along with the inline assembler code. In these examples, however, the result of the expression is computed by the compiler at compile-time, so the expression is optimized away.
3.3.3 The encache.c file

The encache.s file can be found at:

http://www.arm.com/Documentation/AppNotes/code/an53.zip
4 ARMulator

4.1 Introduction

The ARMulator provides a debugging and benchmarking platform for software development. For full details on the ARMulator, refer to:

- *Software Development Toolkit Reference Guide* (ARM DUI 0041), *Chapter 9 The ARMulator*
- *Software Development Toolkit User Guide* (ARM DUI 0040), *Chapter 5 The ARMulator*
- *Application Note 32: The ARMulator* (ARM DAI 0032)
- *Application Note 51: ARMulator Cache Models* (ARM DAI 0051)

This Application Note refers to the Page Tables model.

In releases up to and including release 2.11 of the toolkit, the Page Tables model only supports MMU-based processors. However, it defines memory in terms of regions, in a similar way to the Protection Unit, with the following differences:

- Regions must be multiples of 1MB in size (but may be any integer multiple)
- Regions must lie on any megabyte boundary, rather than one dictated by the region size
- The priority of regions applies ($\text{Region}[1]$ has priority over $\text{Region}[0]$, and so on).

On every reset the Page Tables model:

- Writes a set of page tables to memory
- Sets up the MMU, configuring
  - the page tables base address
  - the Domain Access Control register
- Flushes the cache and TLB
- Enables the cache, write-buffer and MMU (or not, according to the configuration).

4.2 The armul.cnf file

The Page Tables model is configured using the ARMulator configuration file \texttt{armul.cnf}. For fuller details of \texttt{armul.cnf} refer to *Application Note 52: The ARMulator Configuration File* (ARM DAI 0052).

To modify the configuration, locate the \texttt{PageTables} region of the file. This declares the default options for the MMU, and several regions of memory. Details on configuring the model are given in the *Software Development Toolkit User Guide* (ARM DUI 0040), 5.11 Supplied Models: Page Table Manager.

A sample configuration is given for the memory map defined in 3.1 Memory layout on page 4. The sample regions are generated using the same three regions as the Protection Unit example.
In release 2.11 of the ARMulator the Page Tables model ignores Region[0]; the rest of the memory defaults to cacheable, bufferable. Either:

- Rename the Regions 1, 2, 3 etc.

Or

- Modify the model source (line 87 of pagetab.c in source\Win32\Armulator [windows] or armsd.tar:armsd/source) and rebuild ARMulator (See Software Development Toolkit User Guide (ARM DUI 0040), Section 5.3 Rebuilding the ARMulator)

4.2.1 Configuration

```plaintext
;; Page tables
{ PageTables
  MMU=Yes
  AlignFaults=No
  Cache=Yes
  WriteBuffer=Yes
  Prog32=Yes
  Data32=Yes
  LateAbort=Yes
  BigEnd=No
  BranchPredict=Yes
  ICache=Yes
  PageTableBase=0xa0000000
  DAC=0x000000003

; region 0 will cover the whole memory, then two
; regions are used to cover the cacheable parts
{ Region[0]
  // background region - not cacheable
  VirtualBase=0
  PhysicalBase=0
  Pages=4096
  Cacheable=No
  Bufferable=No
  Updateable=No
  Domain=0
  AccessPermissions=3
  Translate=Yes
}

{ Region[1]
  // first region - 16MB
  VirtualBase=0
  PhysicalBase=0
  Pages=16
  Cacheable=Yes
  Bufferable=Yes
  Updateable=Yes
  Domain=0
  AccessPermissions=3
  Translate=Yes
}
```


{ Region[2] 
; second region - 1MB 
VirtualBase=0x7ff00000 
PhysicalBase=0x7ff00000 
Pages=1 
Cacheable=Yes 
Bufferable=Yes 
Updateable=Yes 
Domain=0 
AccessPermissions=3 
Translate=Yes 
} 
}