Application Note 128

Logic Tile Flashing LED Example

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Application Note 128
Versatile Logic Tile example design

Release information

The following changes have been made to this Application Note.

Change history

Date	Issue	Change
March 2004	A	First release
January 2006	B	Getting started section added
May 2006	C	Added support for LTXC4VLX Virtex 4 logic tiles
April 2007	D	Added support for LTXC5VLX330 Virtex 5 logic tiles

Proprietary notice

Confidentiality status

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- the document title
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General suggestions for additions and improvements are also welcome.

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1 Introduction to Flashing LED Application

AN128 provides an entry to designing with the logic tile as a standalone platform (if used together with an Integrator/IM-LT1). It is intended to verify that the correct methods are being used for synthesis, place and route, and programming. This example flashes the LEDs, with frequency controlled by the user switch.

1.1 Getting Started

Follow these steps to program the FPGA image in the Logic Tile with the example provided with this application note.

1. Depending on the system you are using plug the Logic Tile on as follows.

   - Standalone – plug the Logic Tile on the IM-LT1.
   - AP – plug the IM-LT1 on the AP Logic module slot and the Logic Tile on the IM-LT1.
   - CP – plug the IM-LT1 on the Core module and the Logic Tile on the IM-LT1.
   - PB926EJ-S – plug the Logic Tile on the Logic Tile slot.
   - EB – plug the Logic Tile on the Logic Tile slot.

2. Fit the CONFIG jumper link/switch on the PB926EJ-S (J32), IM-LT1 (J10) or EB (S1).
3. Connect RVI or Multi-ICE to the to the JTAG ICE connector (PB926EJ-S J31, IM-LT1 J9 or EB J18), or a USB cable to the USB Debug Port (PB926EJ-S J30, EB J16).

4. Check the external supply voltage.

   - Standalone – connect power to the IM-LT1 power terminal connector J9 (3V3 2A, 5V 1A).
   - AP – connect an ATX power supply to J3 on the AP board (200W).
   - CP – connect +12V to J4 on the CP board (positive on center pin, +/-10%, 35W).
   - PB926EJ-S – connect +12V to J28 on the PB926EJS board (positive on center pin, +/-10%, 35W).
   - EB – connect +12V to J28 on the EB board (positive on center pin, +/-10%, 35W).

5. Power-up the boards. The '3V3' and ‘5V’ LEDs should both be lit.
6. If using Multi-ICE, run Multi-ICE Server, press ctrl-L and load the relevant manual configuration file from the \boardfiles\multi-ice directory. Depending on the version of Multi-ICE used it may also be necessary to add new devices to Multi-ICE. Please refer to \boardfiles\irlength_arm.txt for information on how to do this. Please note that Multi-ICE does not support programming of the newer LT-XC4VLX100+ logic tiles.
7. If using the USB connection, ensure that your PC has correctly identified an ARM® RealView™ ICE Micro Edition device is connected to the USB port. If the Windows operating system requires a USB driver to be installed please refer to PB926EJS or EB \boardfiles\USB_Debug_driver\readme.txt.
8. If using Real View ICE (RVI), you must ensure that the RVI unit is powered and has completed its start-up sequence (check the LEDs on the front panel have stopped flashing).

9. You can now run the relevant ‘progcards’ utility for the connection you have prepared above.

   - progcards_multiice.exe for your Multi ICE connection (LT-XC2V4000+ only)
   - progcards_usb.exe for your USB Debug Port connection
   - progcards_rvi.exe for your RealView ICE connection
     When using RVI select the target RVI box you are using.

10. Select the option for the Logic Tile you are using. The utility will report its progress, it may take several minutes to download. A successful configuration download will be terminated with the message “Programming Successful”.
11. Power down the boards.
12. Set the configuration switches to load Logic Tile FPGA image 0 (S2 on the Logic Tile set to all OFF).
13. Remove the CONFIG jumper link, and power-up the boards. Ensure the 'FPGA_OK’ LED is lit.
14. The system will now be fully configured and ready for use.

2 Flashing LED in detail

The example design implements a moving ones pattern display on the logic tile LEDs and if an IM-LT1 is used the pattern is shown on the IM-LT1 LEDs (LED[7:0]). The rate the LEDs flash at is determined by the setting of S1 on the logic tile.

Use S2 to select FPGA image 0 (Set S2[2] OFF and S2[1] OFF) the 'FPGA IMAGE' LED will be OFF. AN128 will then be loaded as the board is powered up.

The VHDL or Verilog source file for the example is in application note AN128 `\logical\` directory. Build scripts are in the `\physical\` directory for synthesis and place and route. The pin and timing constraints file `an128.ucf` and the tool configuration file `bitgen.ut` are also in the `\physical\` directory. These files (and `.edf` file from Synthesis) are used during the place and route to produce the FPGA `.bit` file.

To reprogram the FPGA `.bit` file into the logic tile configuration memory, run the progcards utility located in the application note AN128 `\boardfiles\` directory (see getting started section).