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Change Log

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This describes the AMBA Reset Controller, and its intended use in a typical AMBA system.

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1.1 Overview

The AMBA specification defines a single reset signal, \( BnRES \), which indicates the current reset status of the system.

This document describes the AMBA Reset Controller, which drives the \( BnRES \) signal. See Figure 1-1: Reset controller block diagram.

![Figure 1-1: Reset controller block diagram](image)
1.2 Signal Description

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>BCLK</td>
<td>In</td>
<td>System (bus) clock. This clock times all bus transfers. The clock has two distinct phases—phase 1 in which BCLK is LOW and phase 2 in which BCLK is HIGH.</td>
</tr>
<tr>
<td>POReset</td>
<td>In</td>
<td>Power on reset input. This signal causes a cold reset when HIGH. May be asserted asynchronously to BCLK.</td>
</tr>
<tr>
<td>BnRES</td>
<td>Out</td>
<td>Reset output. This signal indicates the current reset status.</td>
</tr>
</tbody>
</table>

The source of the POReset signal is implementation dependent.
1.3 Signal Timing

Assertion (the falling edge) of \( BnRES \) is asynchronous to \( BCLK \). De-assertion (the rising edge) of \( BnRES \) is synchronous to \( BCLK \), and changes from the falling edge of the clock. See Figure 1-2: \( BnRES \) timing. \( BnRES \) is only asserted during a Power-On Reset condition, caused by the assertion of the \( POReset \) signal.

The \( POReset \) input is an asynchronous input, and may change at any time.

![Figure 1-2: BnRES timing](image-url)
1.4 Use of BnRES

BnRES is used to indicate a reset condition. BnRES is asserted LOW and is used to indicate that all bus and system state should be initialised. This signal is suitable as an asynchronous clear into state machine flip-flops, and for resetting any peripheral register state that requires initialisation.

During reset, the arbiter grants the bus to the default bus master and holds all other grant signals inactive. The decoder negates all select signals, and drives the slave response signals. The decoder drives BWAIT low.
1.5 Bus Reset State Machine

The reset controller consists of a state machine running off the falling edge of BCLK. The bus states are defined in the following sections.

1.5.1 POR—power on reset

This reset initialises all of the system state and ensures that one tristate driver is enabled on the AMBA system bus. Any peripheral state that is initialised on reset is initialised in this state.

The POR state should be preserved by a power on reset cell or controller, until the system bus clock is running and stable, and the system power supply has reached its correct operating voltage (within its allowed limits).

This major reset is forced as an asynchronous startup condition and must be recognised by all master and slave devices on the system bus. This state is exited synchronously to the system clock BCLK. If there is a “clock valid” signal in the system, this should be used in the reset controller to prevent the POR state from being exited until the clock is valid.

1.5.2 INI—initialise

The INI state is used to hold the BnRES signal asserted (LOW) for some extra clock cycles after the POReset signal is deasserted. In the current implementation this state is maintained for at least two clock cycles, but this period can be increased if necessary.

This state, and all others below, are all entered and exited synchronously to the bus clock.

1.5.3 RUN—run mode

RUN is the normal system operation mode: the bus arbiter allocates resources, normal transactions are allowed and the bus clock runs at the normal speed.

1.5.4 Reset state machine graph

The Bus Mode state machine is shown in Figure 1-3: Reset state machine graph. It is clocked on falling BCLK. The BnRES signal directly reflects the bit 0 of the state number shown in the diagram below.

![Figure 1-3: Reset state machine graph](image-url)