ARM 710a Header Card

Reference Guide

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Key

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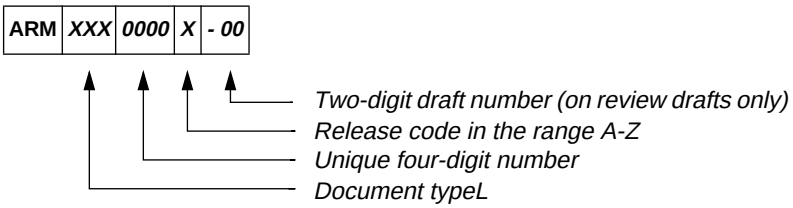

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Advance	Information on a potential product
Preliminary	Current information on a product under development
Final	Complete information on a developed product

Change Log

Issue	Date	By	Change
A	June 97	BJH	First release

EMC Warning

The ARM range of evaluation and development products has been tested for electromagnetic emissions and is restricted to the following guidelines under the EMC directive.

Restrictions on use

- This product should only be used in designated industrial research and development areas.
- It must not be used within 30 metres of a domestic radio or television receiver.
- Mobile phones must not be used within 10 metres of the product.
- ESD precautions must be taken when handling the product.
- Use with a ‘CE’ approved power supply.
- Modifications to these evaluation cards not approved by ARM may cause harmful interference.
- The card should be powered down when not in use.

This equipment generates electromagnetic interference. If not installed and used as directed it may interfere with radio communications and other electronic equipment. If interference is experienced the user should attempt to correct the interference by one or more of the following actions.

Suggested measures for improvement

- Increase the separation distance between the two items.
- Reorient or relocate either item.
- Connect the equipment to different power circuits.
- Use filtered mains plugs or sockets.
- Ensure attached cables do not lie across the card.
- Fit RFI suppression kit which is obtainable from ARM.

Contents

1 ATM710a Header Card

The ARM710a Header Card is a processor daughter board for the ARM Development Board (HBI-0016B). Used in conjunction with this board, the header card is suitable for code development and evaluation of the ARM710a processor.

The header card provides an interface to the Advanced Microcontroller Bus Architecture (AMBA) Advanced System Bus (ASB).

Using the Angel debug monitor program supplied with the card, you can download and run code with the ARM Software Development Toolkit.

ATM710a Header Card

1.1 Programmers' Information

The programmer can consider the header card as an ARM710a processor; this is a general-purpose 32-bit microprocessor with:

- 8Kb cache
- enlarged write buffer
- Memory Management Unit (MMU).

The CPU within a ARM710a is the ARM7.

The ARM710a is software-compatible with the ARM processor family. Please refer to the *ARM710a Macrocell Datasheet (ARM DDI 0033)* for further information.

1.2 Setting up the System

The header card plugs into the top left-hand corner of the development board, with the copyright notice of the header card to the top, so that the header is flush with the development board.

Note *The ARM710a Header card does not provide EmbeddedICE support. To use the Angel Debug Monitor, a serial/parallel link or ethernet connection to the host debugging system is required.*

The host should also be running the ARM debugger (ADW or armsd), which is a program supplied as part of the ARM Software Development Toolkit.

Please refer to the manual *Target Development System User Guide (ARM DUI 0061)* for information on how to establish a debug link between the board and the host system.

1.3 Configuring the ARM710a Header Card

A socket is provided to allow a standard (DIL14 outline) or small (DIL8 outline) crystal oscillator to plug into the header card. A 32MHz crystal oscillator is fitted as default.

The position of a switch on the card determines the source of clock to be used for clocking the core of the ARM710a. The two positions marked on the silkscreen of the board, are:

STB MODE Standard Bus Mode.
Where the core clock is provided by the crystal oscillator, the frequency must be greater or equal to memory interface clock (normally 20 MHz) provided by the motherboard. The memory interface clock frequency is configurable; for details, refer to the *Target Development System User Guide (ARM DUI 0061)*.

FBMODE Fast Bus Mode.
The core is clocked from the memory interface clock which is provided by the motherboard.

Note *Please see the release note supplied with the board for details of the maximum frequency of operation.*

1.3.1 Links

For normal operation, the surface mount links should not be moved. They are set as follows:

LK1	AMBA Bus Master Veneer Configuration	link set between A-C
LK2	AMBA Bus Master Veneer Configuration	link set between B-C
LK3	AMBA Bus Master Veneer Configuration	link set between A-C
LK4	GNT SELECT	default link set between A-C
LK5	REQARM SELECT	default link set between A-C

These links are fitted at factory.

Links 1-3 should not be moved

Links 4 and 5 can be changed over so the links are set between B-C. This allows a second board to plug on top, creating a dual-processor development card, with two boards stacked on top of each other.

Link	Selection	Position
LK4	GNT_ARM = S_GNTARM GNT_ARM = GNT001	A - C B - C
LK5	REQARM = S_REQARM REQARM = REQ001	A - C B - C

Table 1-1: Links 4 and 5

1.3.2 Wire link

The wire link (WL1) on the board is provided for current measurement of the core of the processor. The wire link can be removed and allows an external supply to be introduced, and an ammeter to measure the current.

1.4 Circuit Descriptions

The header card consists of:

- the ARM710a processor
- a switch to set the clocking mode
- a crystal oscillator to provide the core clock, when operating in standard mode
- five buffer chips for improved address and control drive
- a MACH complex programmable logic device (CPLD) implementing an AMBA Bus Master veneer

1.4.1 AMBA bus master veneer

In order to turn the ARM710a processor into an AMBA bus master, an AMBA veneer is required. The function is performed by the MACH215 device (U4). Because this is a 5V part, it is necessary to level-shift the outputs so that output high voltages do not damage the processor. The two level converters (U2 and U3) are constructed from "Quickswitch" buffers. These devices have very low propagation delay (less than 250ps) and appear as a 5 ohm resistor when switched on.

The output voltage for an input voltage equal to the supply is approximately 1V below the supply. A resistor/diode network (R20 and D1) is used to provide a supply of 4.3v, so that high inputs are clamped to 3.3v when driven out of the device.

1.4.2 Header connectors

The schematics show four 60-way connectors (SK1-SK4) which are used to attach all the AMBA bus signals from the header card to the development card.

1.4.3 Processor in QFP

The ARM710a processor is supplied in 144-pin PQFP package; a number of inputs are tied to default values through resistors.

A 32MHz crystal oscillator is supplied on the board. Exact maximum frequency varies with 710a processor manufacturer; please see the release note supplied with the product.

1.4.4 Board schematics

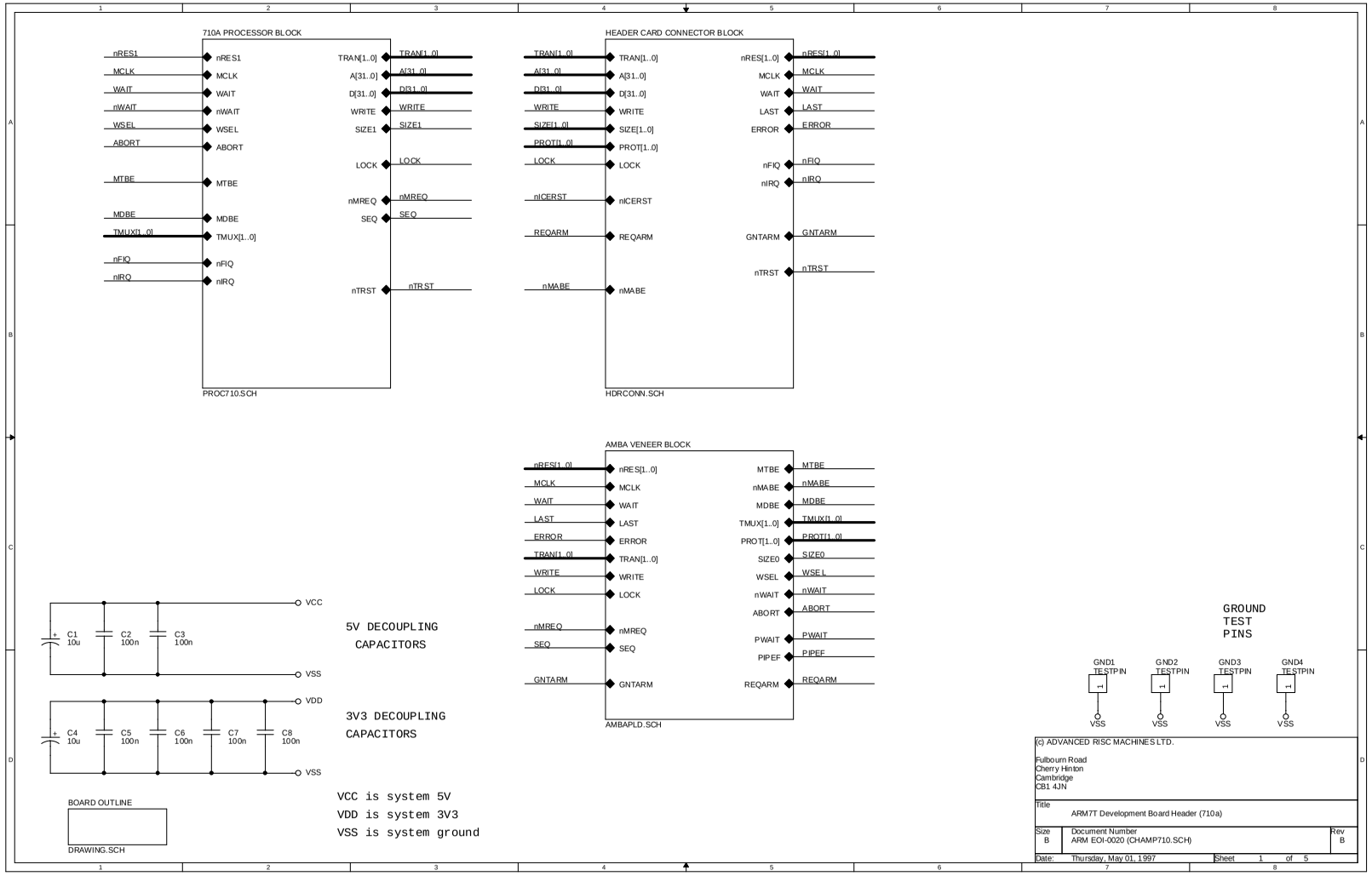
The ARM710a header card design comprises the five schematics listed below.

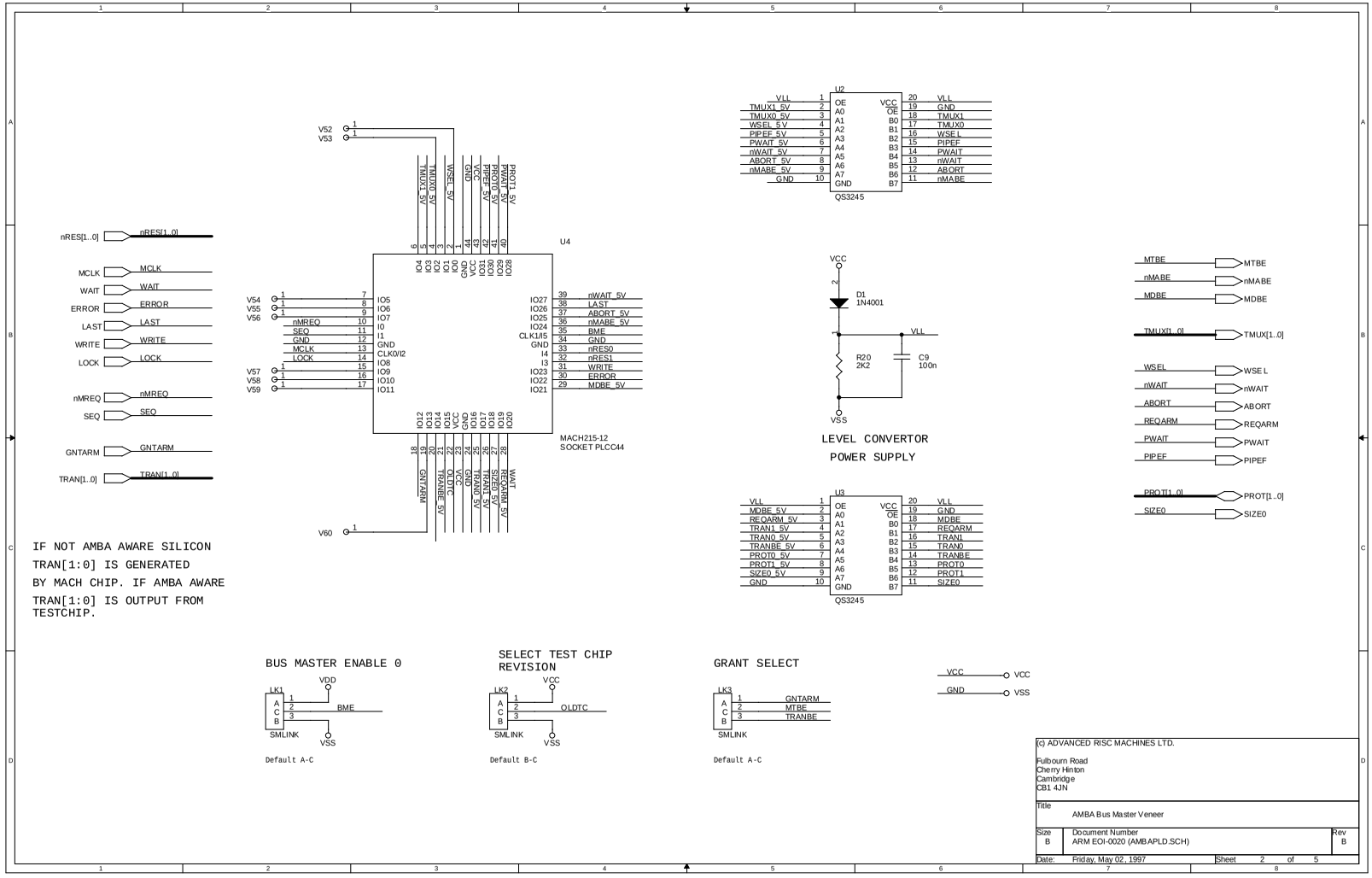
1	Top-level diagram	CHAMP710.SCH
2	AMBA bus master veneer	AMBAPLD.SCH
3	ARM710a processor	PROC710.SCH
4	AMBA header connectors	HDRCONN.SCH
5	Header card outline drawing	DRAWING.SCH

These are described in ***Chapter 2, Board Schematics***.

2 Board Schematics

The board design comprises five schematics as listed below.


710A PROCESSOR BLOCK
nRES1
MCLK
WAIT
nWAIT
WSEL
ABORT
MTBE
MDBE
TMUX[1..0]
nFIQ
nIRQ
TRAN[1..0]
A[31..0]
D[31..0]
WRITE
SIZE1
LOCK
nMREQ
SEQ
nTRST
PROC710.SCH
HEADER CARD CONNECTOR BLOCK
TRAN[1..0]
A[31..0]
D[31..0]
WRITE
SIZE[1..0]
PROT[1..0]
LOCK
nICERST
REQARM
nMABE
nRES[1..0]
MCLK
WAIT
LAST
ERROR
nFIQ
nIRQ
GNTARM
nTRST
HDRCONN.SCH
AMBA VENEER BLOCK
nRES[1..0]
MCLK
WAIT
LAST
ERROR
TRAN[1..0]
WRITE
LOCK
nMREQ
SEQ
GNTARM
MTBE
nMABE
MDBE
TMUX[1..0]
PROT[1..0]
SIZE0
WSEL
nWAIT
ABORT
PWAIT
PIPEF
REQARM
AMBAPLD.SCH
VCC
C1 10u
C2 100n
C3 100n
VSS
5V DECOUPLING CAPACITORS
VDD
C4 10u
C5 100n
C6 100n
C7 100n
C8 100n
VSS
3V3 DECOUPLING CAPACITORS
BOARD OUTLINE
DRAWING.SCH
VCC is system 5V
VDD is system 3V3
VSS is system ground
GROUND TEST PINS
GND1 TESTPIN
GND2 TESTPIN
GND3 TESTPIN
GND4 TESTPIN
VSS
(c) ADVANCED RISC MACHINES LTD.
Fulbourn Road
Cherry Hinton
Cambridge
CB1 4JN
Title
ARM7T Development Board Header (710a)
Size B
Document Number
ARM EOI-0020 (CHAMP710.SCH)
Rev B
Date: Thursday, May 01, 1997
Sheet 1 of 5


U4
MACH215-12
SOCKET PLCC44
U2
QS3245
U3
QS3245
D1
1N4001
R20
2K2
C9
100n
LEVEL CONVERTOR
POWER SUPPLY
IF NOT AMBA AWARE SILICON
TRAN[1:0] IS GENERATED
BY MACH CHIP. IF AMBA AWARE
TRAN[1:0] IS OUTPUT FROM
TESTCHIP.
BUS MASTER ENABLE 0
SELECT TEST CHIP
REVISION
GRANT SELECT
Default A-C
Default B-C
Default A-C
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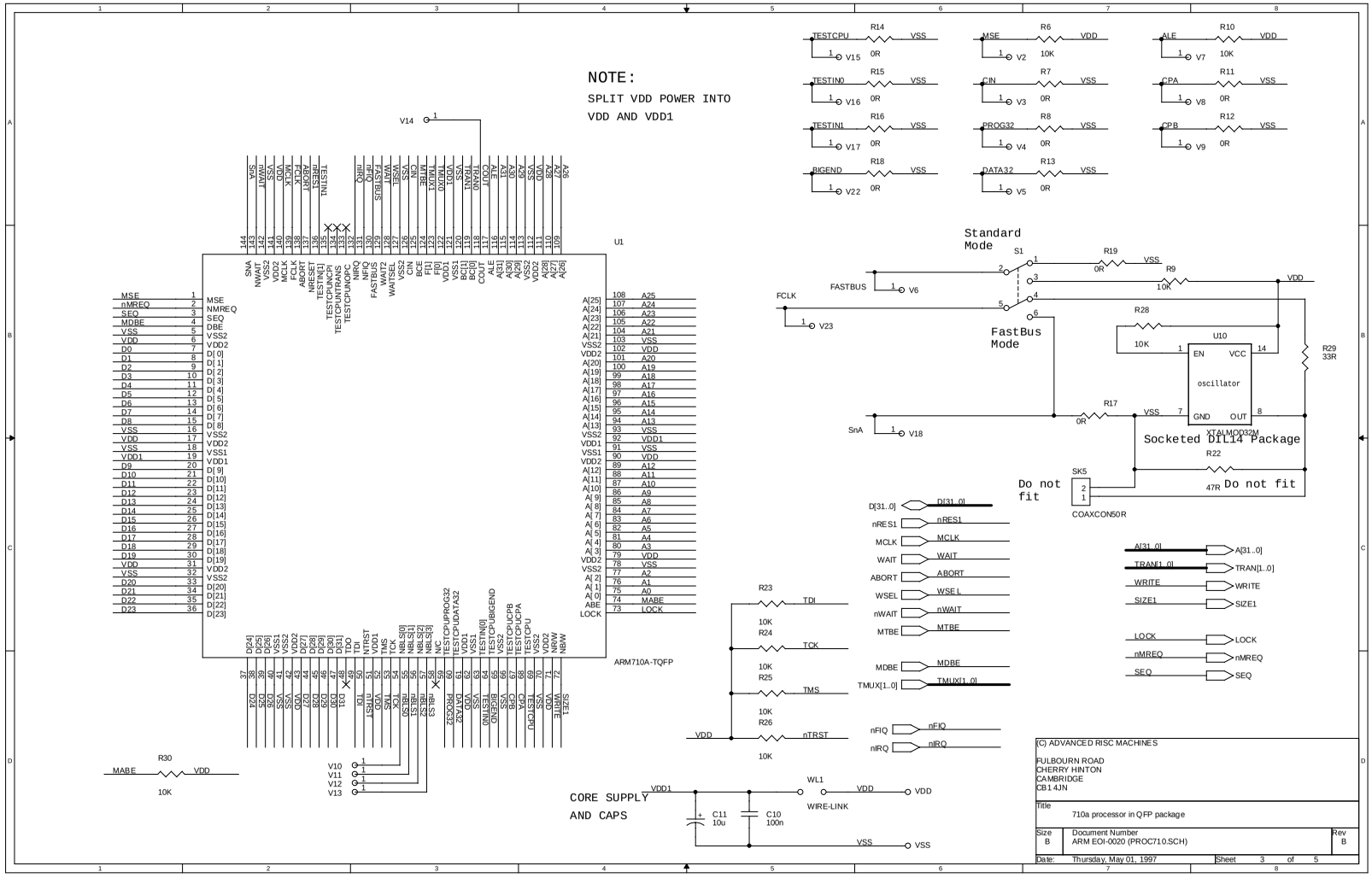
Title
AMBA Bus Master Veneer
Size B
Document Number
ARM EOI-0020 (AMBAPLD.SCH)
Rev B
Date: Friday, May 02, 1997
Sheet 2 of 5


NOTE:
SPLIT VDD POWER INTO
VDD AND VDD1
U1
ARM710A-TQFP
Standard Mode
FastBus Mode
Socketed DIL14 Package
Do not fit
Do not fit
CORE SUPPLY
AND CAPS
WIRE-LINK
oscillator
XTALMOD32M
COAXCON50R
(C) ADVANCED RISC MACHINES
FULBOURN ROAD
CHERRY HINTON
CAMBRIDGE
CB1 4JN
Title
710a processor in QFP package
Size B
Document Number ARM ECI-0020 (PROC710.SCH)
Rev B
Date: Thursday, May 01, 1997
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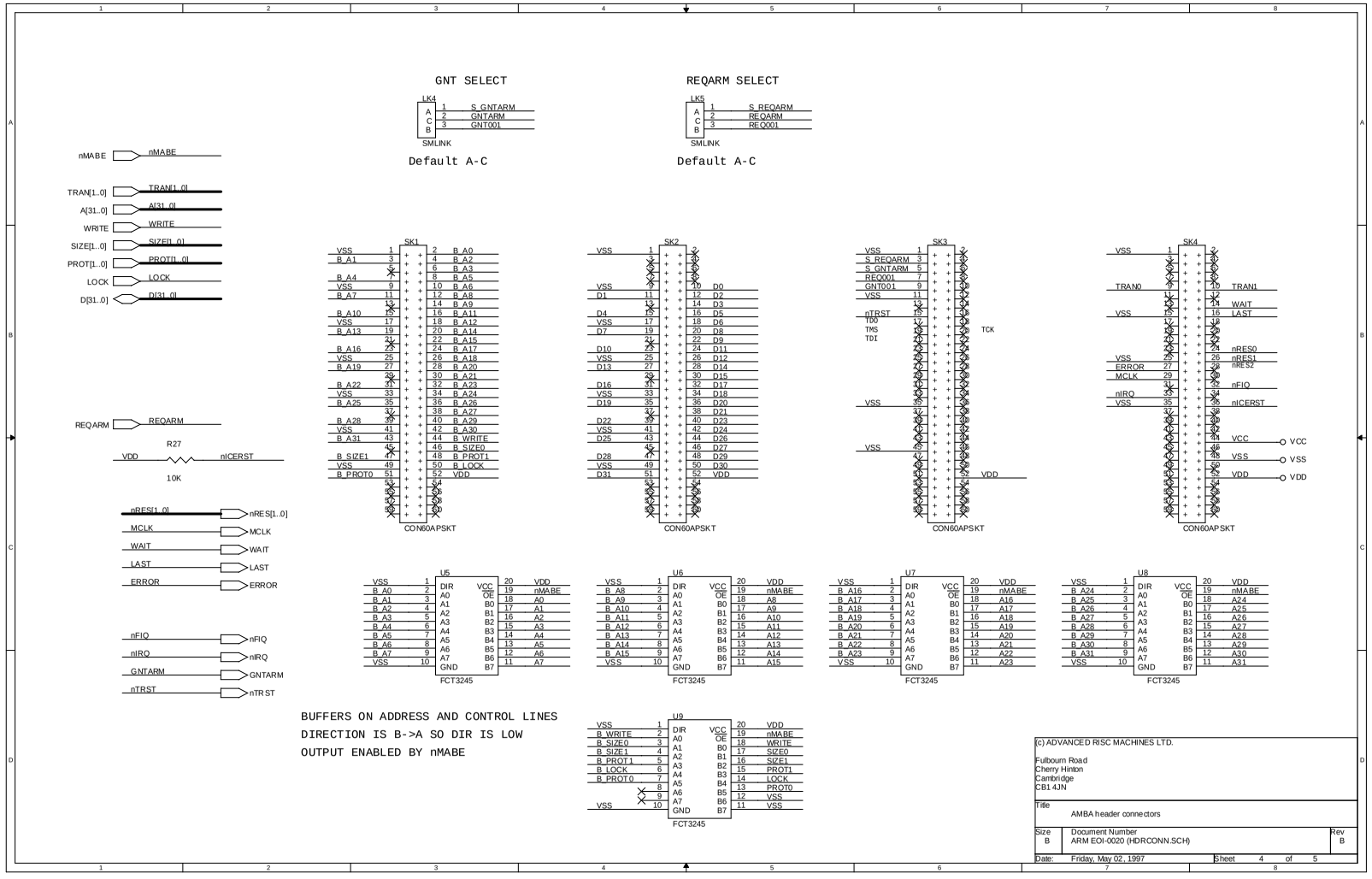
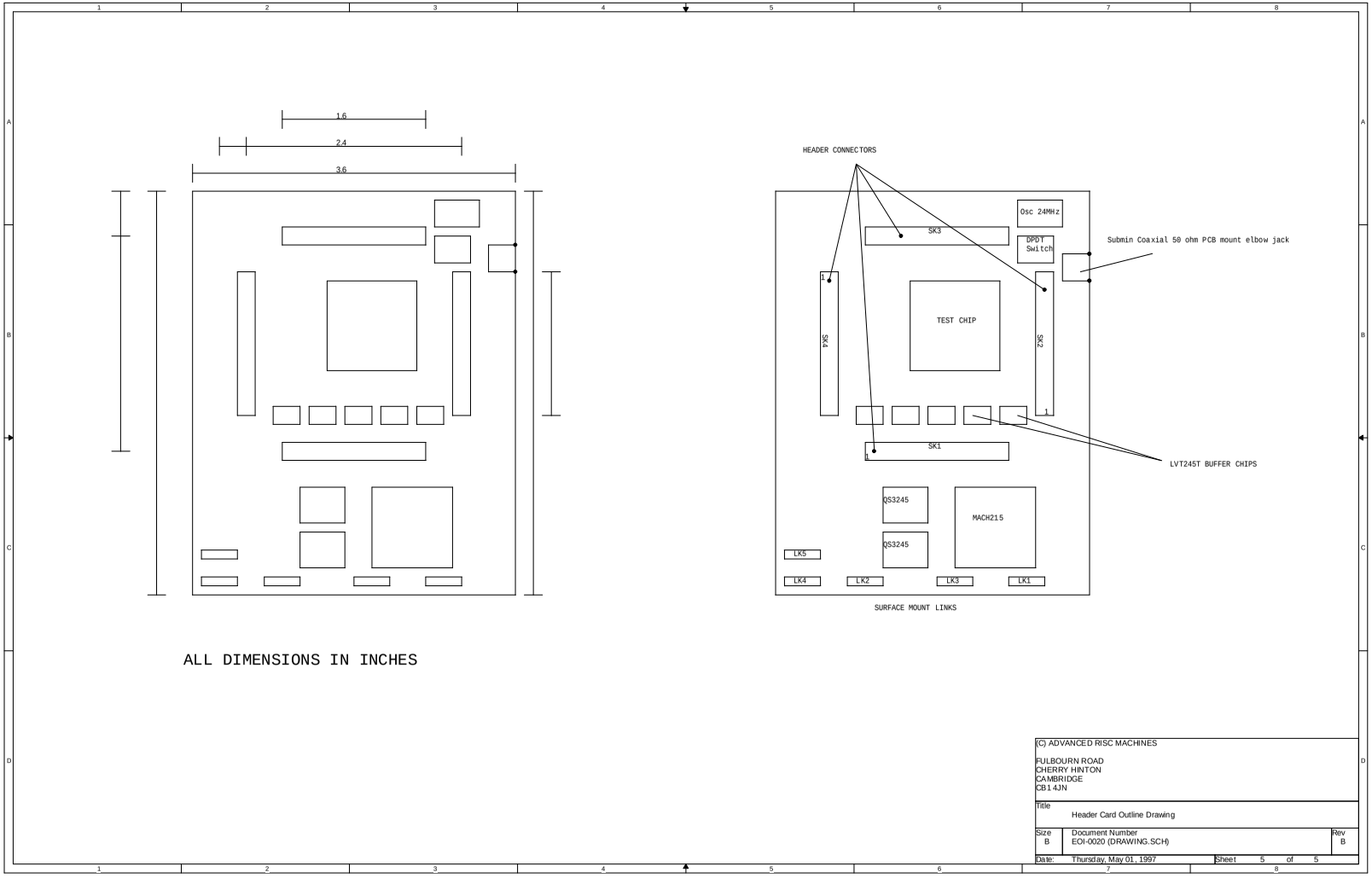

GNT SELECT
LK4
S_GNTARM
GNTARM
GNT001
SMLINK
Default A-C
REQARM SELECT
LK5
S_REQARM
REQARM
REQ001
SMLINK
Default A-C
nMABE
TRAN[1..0]
A[31..0]
WRITE
SIZE[1..0]
PROT[1..0]
LOCK
D[31..0]
REQARM
R27
VDD
nICERST
10K
nRES[1..0]
MCLK
WAIT
LAST
ERROR
nFIQ
nIRQ
GNTARM
nTRST
SK1
SK2
SK3
SK4
CON60APSKT
U5
U6
U7
U8
U9
FCT3245
TCK
VCC
VSS
VDD
BUFFERS ON ADDRESS AND CONTROL LINES
DIRECTION IS B->A SO DIR IS LOW
OUTPUT ENABLED BY nMABE
(c) ADVANCED RISC MACHINES LTD.
Fulbourn Road
Cherry Hinton
Cambridge
CB1 4JN
Title
AMBA header connectors
Size B
Document Number
ARM EOI-0020 (HDRCONN.SCH)
Rev B
Date: Friday, May 02, 1997
Sheet 4 of 5


1.6
2.4
3.6
HEADER CONNECTORS
Osc 24MHz
SK3
DPDT Switch
Submin Coaxial 50 ohm PCB mount elbow jack
TEST CHIP
SK4
SK2
SK1
LVT245T BUFFER CHIPS
QS3245
MACH215
QS3245
LK5
LK4
LK2
LK3
LK1
SURFACE MOUNT LINKS
ALL DIMENSIONS IN INCHES
(C) ADVANCED RISC MACHINES
FULBOURN ROAD
CHERRY HINTON
CAMBRIDGE
CB1 4JN
Title
Header Card Outline Drawing
Size B
Document Number EOI-0020 (DRAWING.SCH)
Rev B
Date: Thursday, May 01, 1997
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