ARM PrimeCell™

DC-DC Converter Interface (PL160)

Technical Reference Manual

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ARM PrimeCell™ DC-DC Converter Interface (PL160) Technical Reference Manual

Release information

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This document is Open Access. This document has no restriction on distribution.

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The information in this document is Final (information on a developed product).

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`http://www.arm.com`

Preface

This preface introduces the ARM PrimeCell DC-DC Converter Interface (PL160) and its reference documentation. It contains the following sections:

- *About this document* on page iv
- *Further reading* on page vii
- *Feedback* on page viii.

About this document

This document is the technical reference manual for the ARM PrimeCell DC-DC Converter Interface (PL160).

Intended audience

This document has been written for experienced hardware and software engineers who may or may not have experience of ARM products.

Organization

This document is organized as follows:

Chapter 1 *Introduction*

Read this chapter for an introduction to the PrimeCell DC-DC Converter Interface and its features.

Chapter 2 *Functional Overview*

Read this chapter for a description of the major functional blocks of the PrimeCell DC-DC Converter Interface.

Chapter 3 *Programmer's Model*

Read this chapter for a description of the PrimeCell DC-DC Converter Interface registers and programming details.

Chapter 4 *Programmer's Model for Test*

Read this chapter for a description of the logic in the PrimeCell DC-DC Converter Interface for functional verification and production testing.

Appendix A *ARM PrimeCell DC-DC Converter Interface (PL160) Signal Descriptions*

Read this appendix for details of the PrimeCell DC-DC Converter Interface signals.

Typographical conventions

The following typographical conventions are used in this document:

bold Highlights signal names within text, and interface elements such as menu names. May also be used for emphasis in descriptive lists where appropriate.

italic Highlights special terminology, cross-references and citations.

`typewriter` Denotes text that may be entered at the keyboard, such as commands, file names and program names, and source code.

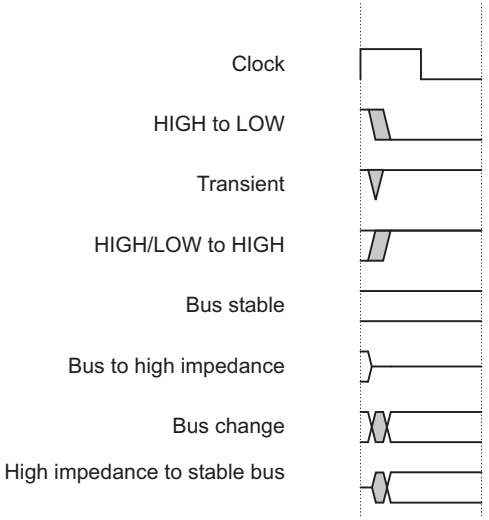
`type`writer Denotes a permitted abbreviation for a command or option. The underlined text may be entered instead of the full command or option name.

`typewriter italic`
Denotes arguments to commands or functions where the argument is to be replaced by a specific value.

`typewriter bold`
Denotes language keywords when used outside example code.

Timing diagram conventions

This manual contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.



Key to timing diagram conventions

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

Further reading

This section lists publications by ARM Limited that are related to this product.

ARM publications

AMBA Specification (Rev 2.0) (ARM IHI 0011).
ARM PrimeCell DC-DC Converter Interface (PL160) Design Manual (PL160 DDES 0000).
ARM PrimeCell DC-DC Converter Interface (PL160) Integration Manual (PL160 INTM 0000).

Feedback

ARM Limited welcomes feedback both on the ARM PrimeCell DC-DC Converter Interface (PL160), and on the documentation.

Feedback on this document

If you have any comments on this document, please send email to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the ARM PrimeCell DC-DC Converter Interface (PL160)

If you have any comments or suggestions about this product, please contact your supplier giving:

- the product name
- a concise explanation of your comments.

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Chapter 1
Introduction

This chapter introduces the ARM PrimeCell DC-DC Converter Interface (PL160) and contains the following sections:

- *About the ARM PrimeCell DC-DC Converter Interface (PL160)* on page 1-2
- *AMBA compatibility* on page 1-4.

1.1 About the ARM PrimeCell DC-DC Converter Interface (PL160)

The PrimeCell DC-DC Converter Interface is an *Advanced Microcontroller Bus Architecture* (AMBA) compliant System-on-a-Chip peripheral that is developed, tested and licensed by ARM.

The PrimeCell DC-DC Converter Interface is an AMBA slave module, and connects to the *Advanced Peripheral Bus* (APB). The PrimeCell DC-DC Converter Interface can be used to implement a configurable dual-output, *Pulse Width Modulation* (PWM) power converter. Figure 1-1 illustrates a typical interconnection scheme for a PWM controller using the PrimeCell DC-DC Converter Interface.

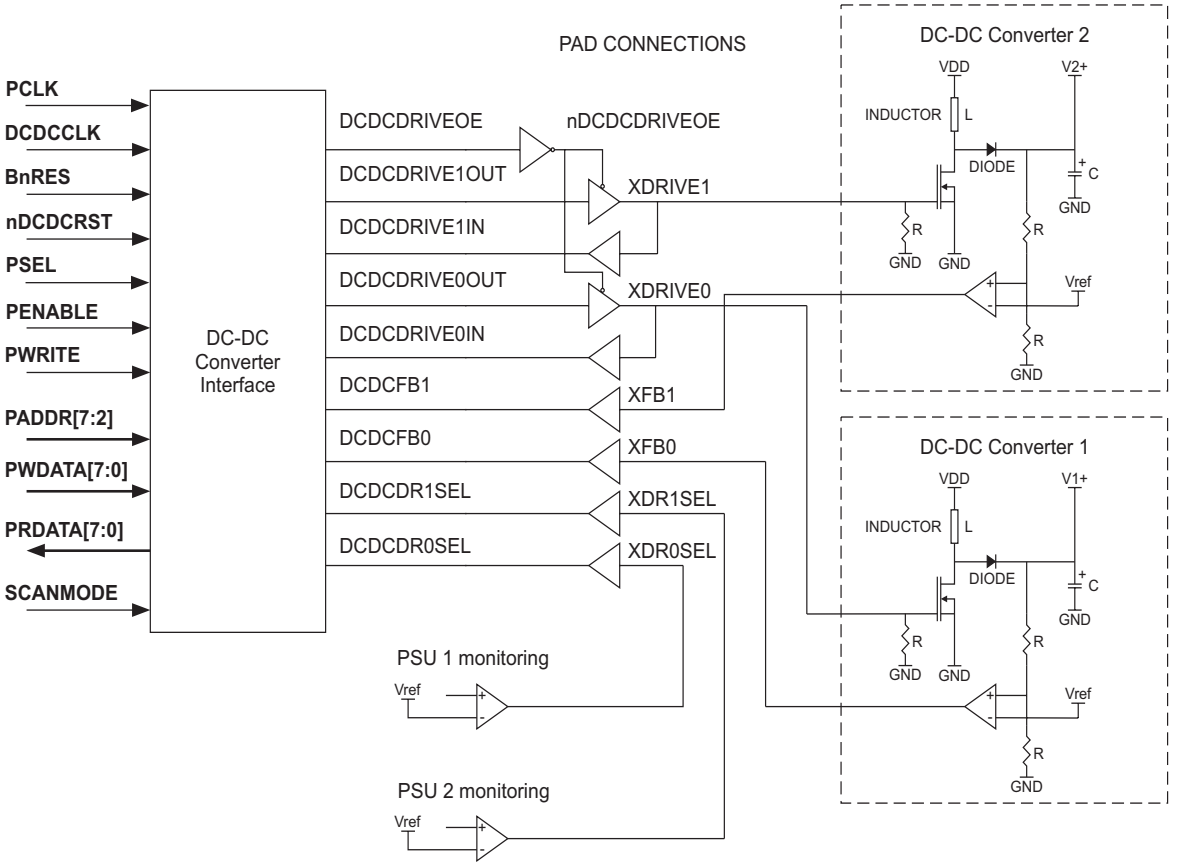

Figure 1-1 PrimeCell DC-DC Converter Interface connections diagram

1.1.1 Features of the PrimeCell DC-DC Converter Interface

The features of the PrimeCell DC-DC Converter Interface are:

- Compliance to the *AMBA Specification (Rev 2.0)* onwards for easy integration into *System-on-a-Chip* (SoC) implementation.
- Dual PWM drive outputs, with independent closed loop feedback.
- Software programmable configuration of one of four output frequencies (each being a fixed divide of the input clock). The selectable divide factors are 16, 32, 128, or 304.
- Software programmable configuration of duty cycle from 0 to $^{15}/_{16}$, in intervals of $^{1}/_{16}$.
- Output polarity (that is, positive or negative voltage generation) is hardware-configured during power-on reset via the polarity select inputs.
- Each PWM drive output can be dynamically switched to one of a pair of preprogrammed frequency/duty cycle combinations via external pins.

1.2 AMBA compatibility

The PrimeCell DC-DC Converter Interface complies with the *AMBA Specification (Rev 2.0)* onwards. The fundamental differences from the *AMBA Specification Revision D* are:

- the timing of the strobe signal **PSTB** compared with the enable signal **PENABLE**
- the time at which read data is sampled
- a separate unidirectional read data bus **PRDATA**, and unidirectional write bus **PWDATA** (instead of the bidirectional data bus **PD**)
- the address bus is named **PADDR** (instead of **PA**).

This document assumes little-endian memory organization, where bytes of increasing significance are stored in increasing addresses in memory, and hence low-order bytes are transferred on the low-order bits of the data bus. Options for a big-endian system are described in the *ARM PrimeCell DC-DC Converter Interface (PL160) Integration Manual*.

Chapter 2
Functional Overview

This chapter describes the major functional blocks of the ARM PrimeCell DC-DC Converter Interface (PL160) and contains the following sections:

- *ARM PrimeCell DC-DC Converter Interface (PL160) overview* on page 2-2
- *PrimeCell DC-DC Converter Interface functional description* on page 2-3
- *PrimeCell DC-DC Converter interface operation* on page 2-6.

2.1 ARM PrimeCell DC-DC Converter Interface (PL160) overview

The PrimeCell DC-DC Converter Interface is a dual-output *Pulse Width Modulation* (PWM) controller. It can be configured under software control by writing control data via the AMBA APB interface to configure frequency and duty cycle of each output.

The two outputs **DCDCDRIVE0OUT** and **DCDCDRIVE1OUT**, can be configured to switch at one of four fixed frequencies with a duty cycle varying from 0 to $^{15}/_{16}$ in increments of $^{1}/_{16}$.

The module requires a clock signal to be applied to the **DCDCCLK** input since there is no internal oscillator. The **DCDCCLK** is internally divided by fixed factors of 16, 32, 128, or 304. If, for example, **DCDCCLK** is driven with a 28.8MHz nominal frequency, then the selectable drive output frequencies will be 1.8MHz, 900kHz, 225kHz, or 94.7kHz respectively.

This module can be used to implement a DC-DC converter by using the outputs to drive external power MOSFETs in an appropriate power conversion circuit.

The **DCDCDRIVE0OUT** and **DCDCDRIVE1OUT** pulses are enabled by the **DCDCFB0** and **DCDCFB1** power supply monitor feedback pins.

During power-on reset, the **DCDCDRIVE0OUT** and **DCDCDRIVE1OUT** outputs are forced into a high-impedance state. Whilst in this state, the outputs are driven by weak pull-up or pull-down resistors and these values are registered to determine the subsequent drive polarity in each case. Registered LOW values will result in positive pulses, whilst registered HIGH values will result in negative pulses appearing on the respective drive output signals.

It is also possible for each drive output to switch between a pair of preprogrammed frequency/duty cycle combinations. To accomplish this, the external signals **DCDCR0SEL** and **DCDCDR1SEL** select one of two frequency and duty cycle configurations for each drive output.

2.2 PrimeCell DC-DC Converter Interface functional description

A block diagram of the PrimeCell DC-DC Converter Interface is shown in Figure 2-1:

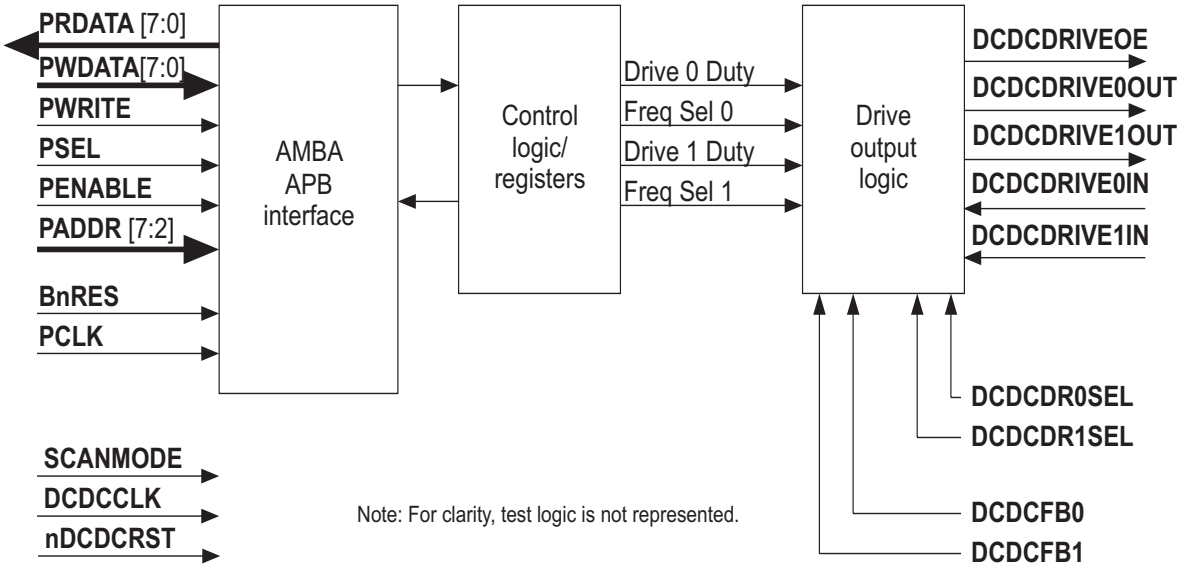

Figure 2-1 PrimeCell DC-DC Converter Interface block diagram

The functions of the PrimeCell DC-DC Converter Interface are described in the following sections:

- *AMBA APB interface*
- *Control logic* on page 2-4
- *Drive output logic* on page 2-5
- *Synchronizing registers and logic* on page 2-5
- *Test registers and logic* on page 2-5.

2.2.1 AMBA APB interface

The AMBA APB interface generates read and write decodes for accesses to status and control registers (see Figure 2-2 on page 2-4 and Figure 2-3 on page 2-4).

The AMBA APB is a local secondary bus which provides a low-power extension to the higher bandwidth AMBA *Advanced High-Performance Bus* (AHB), or AMBA *Advanced System Bus* (ASB), within the AMBA system hierarchy. The AMBA APB groups narrow-bus peripherals to avoid loading the system bus. It provides an interface using memory-mapped registers which are accessed under programmed control.

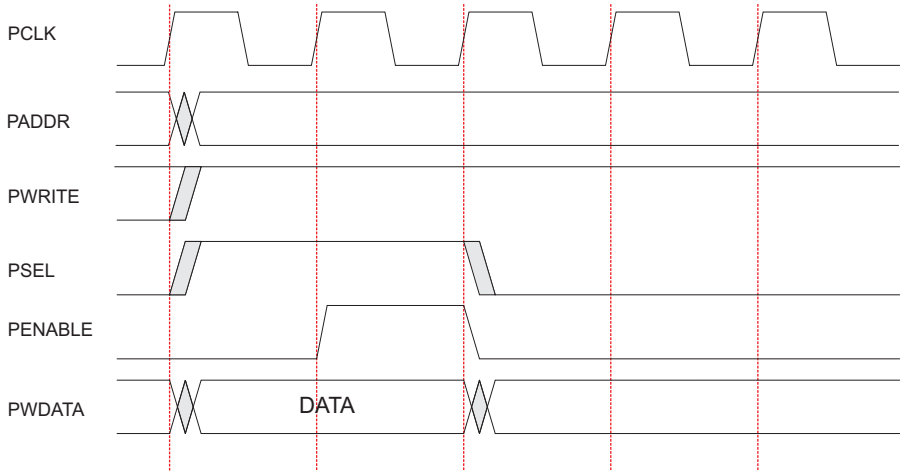

Figure 2-2 AMBA APB write access

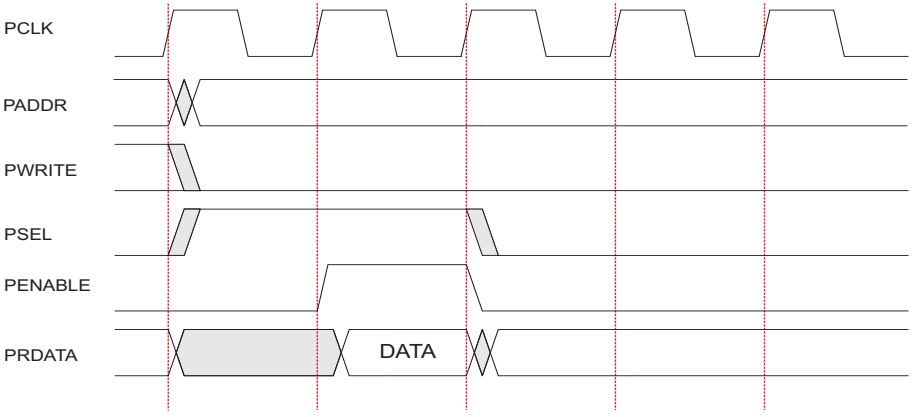

Figure 2-3 AMBA APB read access

2.2.2 Control logic

The control logic block contains normal and test mode registers which store data written across the AMBA APB. The read/write registers also allow data to be read back on the AMBA APB.

2.2.3 Drive output logic

The drive output logic block converts the duty cycle and frequency coefficients supplied by the control block, into the pulse-width modulated outputs, **DCDCDRIVE0OUT** and **DCDCDRIVE1OUT**. This conversion is performed in two stages:

- frequency cycle logic
- duty cycle logic.

In addition to the registers, this block also contains control logic to multiplex the duty cycle and frequency selection for each drive output.

2.2.4 Synchronizing registers and logic

The PrimeCell DC-DC Converter Interface supports both asynchronous and synchronous operation of the clocks, **PCLK** and **DCDCCLK**. Synchronization registers and handshaking logic have been implemented, and are active at all times. This has a minimal impact on performance or area. Synchronization of control signals is performed on both directions of data flow, that is from the **PCLK** to the **DCDCCLK** domain, and **DCDCCLK** to **PCLK**.

2.2.5 Test registers and logic

There are registers and logic for functional block verification, and manufacturing/ production test using TICTalk vectors.

Test registers should not be accessed during normal use.

The test logic allows generation of a special test clock enable signal to propagate the test vectors applied to the input signal of the block and capture values at the block outputs.

2.3 PrimeCell DC-DC Converter interface operation

The operation of the PrimeCell DC-DC Converter Interface is described in the following sections:

- *Interface reset*
- *Clock signals*
- *DC-DC external signals* on page 2-6.

2.3.1 Interface reset

The PrimeCell DC-DC Converter Interface is reset by the global reset signal **BnRES** and a block-specific reset signal **nDCDRST**. An external reset controller must use **BnRES** to assert **nDCDRST** asynchronously and negate it synchronously to **DCDCCLK**. **BnRES** must be asserted LOW for a period long enough to reset the slowest block in the on-chip system, and then be taken HIGH again. The PrimeCell DC-DC Converter Interface requires **BnRES** to be asserted for at least one period of **PCLK** and **nDCDRST** to be asserted for at least one period of **DCDCCLK**.

The values of the registers after reset are decribed in Chapter 3 *Programmer's Model*.

2.3.2 Clock signals

The PrimeCell DC-DC Converter Interface has two input clock signals, **PCLK** and **DCDCDCLK**.

The **DCDCCLK** frequency value should be selected to be 16 times the maximum drive switching frequency that is required on the outputs DCDCDRIVE0OUT and DCDCDRIVE1OUT.

DCDCCLK can be driven by the **PCLK** signal when the frequency value is suitable for the output switching frequency that is required on the outputs. However, separate clock signals are often required due to other system constraints. **DCDCCLK** may be greater or less than the frequency of **PCLK**.

2.3.3 DC-DC external signals

The PrimeCell DC-DC Converter Interface requires the following connections to the external input and bidirectional input/output pads:

- *DCDCDRIVEOE* on page 2-7
- *DCDCDRIVE0OUT, DCDCDRIVE1OUT* on page 2-7
- *DCDCDRIVE0IN, DCDCDRIVE1IN* on page 2-7
- *DCDCFB0, DCDCFB1* on page 2-7
- *DCDCDR0SEL, DCDCDR1SEL* on page 2-7.

DCDCDRIVEOE

DCDCDRIVEOE is a bidirectional external input/output pad enable (active HIGH).

DCDCDRIVE0OUT, DCDCDRIVE1OUT

DCDCDRIVE0OUT, DCDCDRIVE1OUT are drive outputs that feed data values through to the outputs of the bidirectional input/output pads. These drive outputs switch according to their programmed frequency and duty cycle, and the state of the select inputs **DCDCDR0SEL** and **DCDCDR1SEL**. The polarity of the drive output depends on the state of the captured input values of **DCDCDRIVE0IN** and **DCDCDRIVE1IN** during reset. The drive outputs are enabled if the external feedback inputs **DCDCFB0** and **DCDCFB1** are asserted HIGH, otherwise the drive outputs are negated when the feedback inputs are LOW.

DCDCDRIVE0IN, DCDCDRIVE1IN

DCDCDRIVE0IN, DCDCDRIVE1IN are drive inputs fed from bidirectional input/output pads. The state of the drive input during reset determines the polarity of the drive output. The two possible conditions are detailed in Table 2-1.

Table 2-1 Setting drive output polarity and converter voltage polarity

State of DCDCDRIVExIN during reset	Drive output polarity	Converter voltage polarity
LOW	Active HIGH	Positive
HIGH	Active LOW	Negative

DCDCFB0, DCDCFB1

DCDCFB0, DCDCFB1 are external feedback drive enable inputs. The drive output is enabled if the feedback input is asserted HIGH. If the feedback input is LOW, then the drive output is negated.

DCDCDR0SEL, DCDCDR1SEL

External drive configuration select inputs. The configuration select inputs are used to select one of two programmed configuration values for the drive output frequency and duty cycle. The input signals could be used for selectable configuration based on the supply source. For example, **DCDCDRxSEL** being HIGH could indicate battery-

powered and **DCDCDRxSEL** being LOW could indicate mains-powered. This would allow different duty cycles for mains/battery operations due to different voltages involved.

The combined effect of capturing the appropriate required polarity and forcing the duty cycle registers to zero during a reset sequence ensures that the external components that complete the DC-DC unit do not draw excessive static current during, or immediately after, removal of the reset signal.

The frequency select bits should be written to the PMPFREQ register to select the output frequency for each drive output.

Four 2-bit values are written to the PMPFREQ register, to select the drive output frequency for each drive output. The 2-bit value selects the frequency output as shown in Table 2-2.

Table 2-2 Frequency selection

Frequency select value (2-bits)	Frequency selected
00	Freq0 = $^{f}/_{16}$
01	Freq1 = $^{f}/_{32}$
10	Freq2 = $^{f}/_{128}$
11	Freq3 = $^{f}/_{304}$

Note that f = Frequency of input clock **DCDCCLK**.

The drive outputs can then be enabled by writing duty cycle values to PMPCON0 and PMPCON1.

Each drive output can be turned off by writing a zero duty cycle value to the appropriate configuration register PMPCON0 or PMPCON1.

Figure 2-4 illustrates an example drive 0 waveform for an active HIGH output, at $^{3}/_{16}$ duty cycle with freq0 ($^{f}/_{16}$) selected.

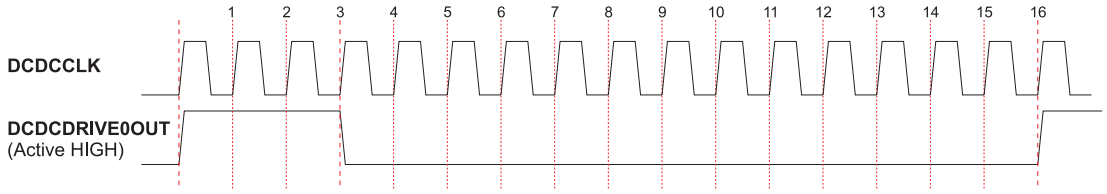

Figure 2-4 Example drive 0 waveform

Chapter 3
Programmer's Model

This chapter describes the ARM PrimeCell DC-DC Converter Interface (PL160) registers and provides details needed when programming the microcontroller. It contains the following sections:

- *About the programmer's model* on page 3-2
- *Summary of PrimeCell DC-DC Converter Interface registers* on page 3-3
- *Register descriptions* on page 3-4.

3.1 About the programmer's model

The base address of the PrimeCell DC-DC Converter Interface is not fixed and may be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

The following locations are reserved, and must not be used during normal operation:

- locations at offsets +0x0c through +0x3c and 0xa4 through 0xff are reserved for possible future extensions
- locations at offsets 0x40 through 0xa0 are reserved for test purposes.

3.2 Summary of PrimeCell DC-DC Converter Interface registers

The PrimeCell DC-DC Converter Interface registers are shown in Table 3-1.

Table 3-1 PrimeCell DC-DC Converter Interface register summary

Address	Type	Width	Reset value	Name	Description
DCDCBase + 0x00	Read/ write	8	0x00	PMPCON0	Drive 0 configuration register.
DCDCBase + 0x04	Read/ write	8	0x00	PMPCON1	Drive 1 configuration register.
DCDCBase + 0x08	Read/ write	8	0x00	PMPFREQ	Frequency configuration register.
DCDCBase + 0x0c-3c	-	-	-	-	Reserved.
DCDCBase + 0x40-a0	-	-	-	-	Reserved (for test purposes).
DCDCBase + 0xa4-ff	-	-	-	-	Reserved.

3.3 Register descriptions

The following registers are described in this section:

- *PMPCON0 [8] (+0x00)*
- *PMPCON1 [8] (+0x04)* on page 3-5
- *PMPFREQ [8] (+0x08)* on page 3-6.

For each of the register descriptions, the format of the title is:

Register name [bit width] (Offset from Base).

3.3.1 PMPCON0 [8] (+0x00)

PMPCON0 is the DC-DC Converter Interface drive 0 configuration register. Two 4-bit values are written to this register to program the drive 0 output duty cycle:

- The upper nibble is selected when the configuration select input **DCDCDR0SEL** is HIGH.
- The lower nibble is selected when the configuration select input **DCDCDR0SEL** is LOW.

The 4-bit duty cycle value 0 to 15 provides a duty cycle from 0 to $^{15}/_{16}$, in intervals of $^{1}/_{16}$. Table 3-2 shows the bit assignments for the PMPCON0.

Table 3-2 PMPCON0 register

Bits	Name	Function
7:4	Drv0DtyHigh	Drive 0 output duty cycle value, selected when input **DCDCDR0SEL** is HIGH. Value 0 to 15 generates duty cycle from 0 to $^{15}/_{16}$, in increments of $^{1}/_{16}$ respectively.
3:0	Drv0DtyLow	Drive 0 output duty cycle value, selected when input **DCDCDR0SEL** is LOW. Value 0 to 15 generates duty cycle from 0 to $^{15}/_{16}$, in increments of $^{1}/_{16}$ respectively.

3.3.2 PMPCON1 [8] (+0x04)

PMPCON1 is the PrimeCell DC-DC Converter Interface drive 1 configuration register. Two 4-bit values are written to this register to program the drive 1 output duty cycle:

- The upper nibble is selected when the configuration select input **DCDCDR1SEL** is HIGH.
- The lower nibble is selected when the configuration select input **DCDCDR1SEL** is LOW.

The 4-bit duty cycle value 0 to 15 provides a duty cycle from 0 to $^{15}/_{16}$, in intervals of $^{1}/_{16}$. Table 3-3 shows the bit assignments for the PMPCON1.

Table 3-3 PMPCON1 register

Bits	Name	Function
7:4	Drv1DtyHigh	Drive 1 output duty cycle value, selected when input **DCDCDR1SEL** is HIGH. Value 0 to 15 generates duty cycle from 0 to $^{15}/_{16}$, in increments of $^{1}/_{16}$ respectively.
3:0	Drv1DtyLow	Drive 1 output duty cycle value, selected when input **DCDCDR1SEL** is LOW. Value 0 to 15 generates duty cycle from 0 to $^{15}/_{16}$, in increments of $^{1}/_{16}$ respectively.

3.3.3 PMPFREQ [8] (+0x08)

PMPFREQ is the DC-DC Converter Interface frequency configuration register. The value written determines the output frequency for each drive output according to the status of the configuration select input for each drive. Table 3-4 shows the output frequency configuration.

Table 3-4 Output frequency configuration

Bit	Name	Type	Drive output	Configuration select input	Frequency select
7:6	Drv1FreqHigh	Read/ write	1	DCDCR1SEL=HIGH	00 = Freq0 = $^{f}/_{16}$ 01 = Freq1 = $^{f}/_{32}$ 02 = Freq2 = $^{f}/_{128}$ 03 = Freq3 = $^{f}/_{304}$
5:4	Drv1FreqLow	Read/ write	1	DCDCR1SEL=LOW	
3:2	Drv0FreqHigh	Read/ write	0	DCDCR0SEL=HIGH	
1:0	Drv0FreqLow	Read/ write	0	DCDCR0SEL=LOW	

Note that f = Frequency of clock input **DCDCCLK**.

Chapter 4
Programmer's Model for Test

This chapter describes the additional logic for functional verification and production testing. It contains the following sections:

- *PrimeCell DC-DC Converter Interface test harness overview* on page 4-2
- *Scan testing* on page 4-3
- *Test registers* on page 4-4.

4.1 PrimeCell DC-DC Converter Interface test harness overview

The additional logic for functional verification and production testing allows:

- stimulation of input signals to the block
- capture of the output signals
- generation of a special test clock enable signal to propagate test vectors.

These test features are controlled by test registers. This allows testing of the PrimeCell DC-DC Converter Interface in isolation from the rest of the system using only transfers from the AMBA APB.

Off-chip test vectors are supplied via a 32-bit parallel *External Bus Interface* (EBI) and converted to internal AMBA bus transfers. The application of test vectors is controlled via the *Test Interface Controller* (TIC) AMBA bus master module.

During test the **DCDCCLK** signal must be driven by the free-running **PCLK** clock signal so that the test vectors can be frequency independent. This clock multiplexing must be performed externally from the PrimeCell DC-DC Converter Interface. Figure 4-1 shows a block diagram of the PrimeCell DC-DC Converter Interface.

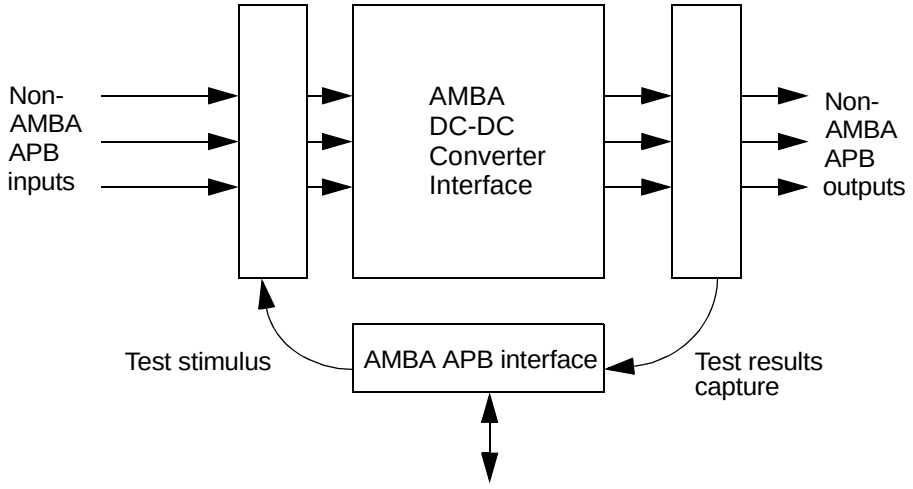

Figure 4-1 PrimeCell DC-DC Converter Interface test harness

4.2 Scan testing

The PrimeCell DC-DC Converter Interface has been designed to simplify insertion of scan test cells and the use of *Automatic Test Pattern Generation* (ATPG) for an alternative method of manufacturing test.

During scan testing, the **SCANMODE** input must be driven HIGH to ensure that all internal data storage elements can be asynchronously reset. For normal use and application of manufacturing test vectors via the TIC, **SCANMODE** must be negated LOW.

4.3 Test registers

The PrimeCell DC-DC Converter Interface test registers are memory-mapped as shown in Table 4-1.

Table 4-1 Test registers memory map

Address	Type	Width	Reset value	Name	Description
DCDCBase + 0x40 -7c	Read/ write	0	-	PMPTCER	Test clock enable register.
DCDCBase + 0x80	Read/ write	5	0x00	PMPTCR	Test control register.
DCDCBase + 0x84	Read/ write	2	0x0	PMPTMR	Test mode register.
DCDCBase + 0x88	Read/ write	6	0x00	PMPTISR	Test input stimulus register.
DCDCBase + 0x8c	Read	3	0x01	PMPTOCR	Test output capture register.
DCDCBase + 0x90	Read	5	0x00	PMPFC0	Frequency counter 0 value read test register.
DCDCBase + 0x94	-	-	-	-	Reserved.
DCDCBase + 0x98	Read	5	0x00	PMPFC1	Frequency counter 1 value read test register.
DCDCBase + 0x9c	-	-	-	-	Reserved.
DCDCBase + 0xa0	Read	8	0x00	PMPDRVCNT	**DCDCDRIVE0OUT** and **DCDCDRIVE1OUT** pulse width generation counter values read test register.

Each register shown in Table 4-1 is described below.

4.3.1 PMPTCER [0] (+0x40-0x7c)

PMPTCER is the test clock enable register. This is a 0-bit register. Table 4-2 shows the bit assignments for the PMPTCER.

Table 4-2 PMPTCER register

Bit	Name	Description
7:0	-	When in registered clock mode (see *PMPTCR [5] (+0x80)* on page 4-5), a test clock enable is produced only when this register is accessed (read or write).

Note

DCDCCLK must be driven by **PCLK** during test. PMPTCER has a multiple word space in the register address map to allow for generation of multiple test clock enable pulses.

4.3.2 PMPTCR [5] (+0x80)

PMPTCR is the test control register. This general test register controls operation of the PrimeCell DC-DC Converter Interface under test conditions. Table 4-3 shows the bit assignments for the PMPTCR.

Table 4-3 PMPTCR register

Bit	Name	Description
7:5	-	Reserved, read unpredictable, should be written as 0.
4	Test Input Select (TESTINPSEL)	This bit is cleared to 0, by default, for normal operation. This bit selects the source for the internal primary inputs (**DCDCFB1**, **DCDCFB0**, **DCDCDRIVE1IN**, **DCDCDRIVE0IN**, **DCDCDR1SEL**, and **DCDCDR0SEL**). 0 = The external primary inputs from pads are used (normal operation). 1 = The values programmed in **PMPTISR** are used on this register for the internal primary inputs instead of the signals from the input/output pads.
3	Test Reset (TESTRST)	When reset by **BnRES**, this bit is cleared to 0 for normal operation, by default. When this bit is set to 1, a reset is asserted throughout the module, *except* for the test registers (this simulates reset by **BnRES** being asserted to 0).

Table 4-3 PMPTCR register (continued)

Bit	Name	Description
2	Registered Clock Mode (REGCLK)	This bit selects the internal test clock mode: 0 = Strobe clock mode is selected. This generates a test clock enable on every APB access (read or write) to the block. Use of strobe clock mode allows testing with less test vectors when testing functions such as counters. The test clock enable is generated from **PENABLE** ANDed with **PSEL**. 1 = Registered clock mode is selected. This only generates a test clock enable on an APB access to the **PMPTCER** (PrimeCell DC-DC Converter Interface test clock enable register) location. This bit has no effect unless bit 0 and bit 1 are both set to 1. When reset by **BnRES**, this bit is cleared to 0 by default.
1	Test Clock Enable (TESTCLKEN)	This bit selects the source of the test clock: 0 = The external free-running **DCDCCLK** and **PCLK** clock inputs are selected, by forcing test clock enable HIGH continuously, enabling the clock on every period of the input clock signals. This is the default value, and it is used for normal operation as well as free running system testing (validation). 1 = The internal test clock enable is selected, so that the test clocks are enabled for only one period of the input clock per APB access. The internal clock enable mode depends on the setting of bit 2. This bit has no effect unless bit 0 is set to 1. When reset by **BnRES**, this bit is cleared to 0 by default.
0	Test Mode Enable (TESTEN)	0 = Normal operating mode is selected. 1 = Test mode is selected. Bits 1 and 2 have no effect unless bit 0 is set to 1. When reset by **BnRES**, this bit is cleared to 0 by default.

4.3.3 PMPTMR [2] (+0x84)

PMPTMR is the test mode register. This test register controls the specific test modes of the PrimeCell DC-DC Converter Interface under test conditions.

All the bits are read as 0 after reset. Table 4-4 shows the bit assignments for the PMPTMR.

Table 4-4 PMPTMR register

Bit	Name	Description
1	Frequency Divider 1 Test Count Enable (TESTCOUNT1)	Setting the bit to 1 enables frequency divider 1 test count enable mode (nibble mode). The test mode enables verification of counter functionality in less clock cycles because the counter is decremented by 0x11 instead of 0x01 as in normal mode. This bit is cleared to 0 for normal operation so that the counter decrements by 1 on each enabled clock cycle.
0	Frequency Divider 0 Test Count Enable (TESTCOUNT0)	Setting the bit to 1 enables frequency divider 0 test count enable mode (nibble mode). The test mode enables verification of counter functionality in less clock cycles because the counter is decremented by 0x11 instead of 0x01 as in normal mode. This bit is cleared to 0 for normal operation so that the counter decrements by 1 on each enabled clock cycle.

4.3.4 PMPTISR [6] (+0x88)

PMPTISR is the test input stimulus register. This register provides direct stimulus control of the PrimeCell DC-DC Converter Interface non-AMBA primary inputs. Table 4-5 shows the bit assignments for the PMPTISR.

Table 4-5 PMPTISR register

Bit	Name	Description
7:6	-	Reserved, read unpredictable, should be written as 0.
5	Rfb1	Programmable test stimulus to primary input **DCDCFB1**.
4	Rfb0	Programmable test stimulus to primary input **DCDCFB0**.
3	RDrive1In	Programmable test stimulus to primary input **DCDCDRIVE1IN**.

Table 4-5 PMPTISR register (continued)

Bit	Name	Description
2	RDrive0In	Programmable test stimulus to primary input **DCDCDRIVE0IN**.
1	Rdrv1Sel	Programmable test stimulus to primary input **DCDCDR1SEL**.
0	Rdrv0Sel	Programmable test stimulus to primary input **DCDCDR0SEL**.

4.3.5 PMPTOCR [3] (+0x8c)

PMPTOCR is the test output capture register (read only). This register provides observation of the PrimeCell DC-DC Converter Interface non-AMBA primary outputs. Table 4-6 shows the bit assignments for the PMPTOCR.

Table 4-6 PMPTOCR register

Bit	Name	Description
7:3		Reserved, unpredictable when read.
2	DCDCDRIVEOE	Test observation for primary output **DCDCDRIVEOE**.
1	DCDCDRIVE1OUT	Test observation for primary output **DCDCDRIVE1OUT**.
0	DCDCDRIVE0OUT	Test observation for primary output **DCDCDRIVE0OUT**.

4.3.6 PMPFC0 [5] (+0x90)

PMPFC0 is the test frequency counter/divider 0 register (read only). It provides an efficient method of monitoring the counter state. Table 4-7 shows the bit assignments for the PMPFCO.

Table 4-7 PMPFC0 register

Bit	Name	Description
4:0	FRQCNT0	DCDC frequency counter 0 register. Reading this register returns the current counter value of the **DCDCDRIVE0OUT** frequency divider.

4.3.7 PMPFC1 [5] (+0x98)

PMPFC1 is the test frequency counter/divider 1 register (read only). It provides an efficient method of monitoring the counter state. Table 4-8 shows the bit assignments for the PMPFC1.

Table 4-8 PMPFC0 register

Bit	Name	Description
4:0	FRQCNT1	DCDC frequency counter 1 register. Reading this register returns the current counter value of the **DCDCDRIVE1OUT** frequency divider.

4.3.8 PMPDRVCNT [8] (+0xa0)

PMPDRVCNT is the test counter register (read only) that returns the values of the counters used to generate **DCDCDRIVE0OUT** and **DCDCDRIVE1OUT** pulse widths. Table 4-9 shows the bit assignments for the PMPTOCR.

Table 4-9 PMPTOCR register

Bit	Name	Description
7:4	DRV1CNT	**DCDCDRIVE1OUT** pulse width counter value. Reading this value returns the current value of the **DCDCDRIVE1OUT** pulse width generator value.
3:0	DRV0CNT	**DCDCDRIVE0OUT** pulse width counter value. Reading this value returns the current value of the **DCDCDRIVE0OUT** pulse width generator value.

Appendix A
ARM PrimeCell DC-DC Converter Interface (PL160) Signal Descriptions

This appendix describes the signals that interface with the ARM PrimeCell DC-DC Converter Interface (PL160). It contains the following sections:

- *AMBA APB signals* on page A-2
- *On-chip signals* on page A-3
- *Signals to pads* on page A-4.

A.1 AMBA APB signals

The PrimeCell DC-DC Converter Interface block is connected to the AMBA APB as a bus slave. With the exception of the **BnRES** signal, the AMBA APB signals have a **P** prefix and are active high. Active low signals contain a lower case **n**. The AMBA APB signals are described in Table A-1.

Table A-1 AMBA APB signal description

Name	Type	Source/ destination	Description
BnRES	Input	Reset controller	Bus reset signal, active LOW.
PADDR [7:2]	Input	APB bridge	Subset of AMBA APB address bus.
PCLK	Input	Clock generator	AMBA APB clock, used to time all bus transfers.
PENABLE	Input	APB bridge	AMBA APB enable signal. **PENABLE** is asserted HIGH for one cycle of **PCLK** to enable a bus transfer.
PRDATA [7:0]	Output	APB bridge	Subset of unidirectional AMBA APB read data bus.
PSEL	Input	APB bridge	PrimeCell DC-DC Converter Interface select signal from decoder. When set to 1 this signal indicates the slave device is selected and that a data transfer is required.
PWDATA [7:0]	Input	APB bridge	Subset of unidirectional AMBA APB write data bus.
PWRITE	Input	APB bridge	AMBA APB transfer direction signal, indicates a write access when HIGH, read access when LOW.

A.2 On-chip signals

A free-running reference clock, **DCDCCLK**, must be provided. By default it is assumed to be asynchronous to **PCLK**.

The **BnRES** and **nDCDCRST** input signals should be asynchronously asserted but synchronously negated to **PCLK** and **DCDCCLK** respectively.

The on-chip signals required in addition to the AMBA APB signals are shown in Table A-2.

Table A-2 On-chip signal descriptions

Name	Type	Source/ destination	Description
DCDCCLK	Input	Clock generator	PrimeCell DC-DC Converter Interface reference clock.
nDCDCRST	Input	Reset controller	PrimeCell DC-DC Converter Interface reset signal to **DCDCCLK** clock domain, active LOW. The reset controller must use **BnRES** to assert **nDCDCRST** asynchronously but negate it synchronously with **DCDCCLK**.
SCANMODE	Input	Test controller	PrimeCell DC-DC Converter Interface scan test hold input. This signal must be asserted HIGH during scan testing to ensure that internal data storage elements can be asynchronously reset. **SCANMODE** must be negated LOW during normal use or when applying manufacturing test vectors via the TIC.

A.3 Signals to pads

Table A-3 describes the signals from the PrimeCell DC-DC Converter Interface block to the input/output pads of the chip. It is the responsibility of the user to make proper use of the peripheral pins to meet the exact interface requirements.

Table A-3 Pad signal descriptions

Name	Type	Source/ destination	Description
DCDCDRIVE0IN	Input	Pad	This input is sampled during reset to determine the drive 0 output polarity of **DCDCDRIVE0OUT**. The output is active HIGH if the input is LOW during reset. The output is active LOW if the input is HIGH during reset.
DCDCDRIVE1IN	Input	Pad	This input is sampled during reset to determine the drive 1 output polarity of **DCDCDRIVE1OUT**. The output is active HIGH if the input is LOW during reset. The output is active LOW if the input is HIGH during reset.
DCDCFB0	Input	Pad	External feedback input from analog circuitry. Drive 0 output **DCDCDRIVE0OUT** is enabled when this input is HIGH. Otherwise, the output is negated.
DCDCFB1	Input	Pad	External feedback input from analog circuitry. Drive 1 output **DCDCDRIVE1OUT** is enabled when this input is HIGH. Otherwise, the output is negated.
DCDCDR0SEL	Input	Pad	External configuration select input. This input selects one of two frequency and duty configurations for drive 0 output **DCDCDRIVE0OUT**.
DCDCDR1SEL	Input	Pad	External configuration select input. This input selects one of two frequency and duty configurations for drive 1 output **DCDCDRIVE1OUT**.
DCDCDRIVE0OUT	Output	Pad	Drive 0 PWM output to control an external power transistor in a DC-DC converter circuit, with a software-programmable frequency and duty cycle.
DCDCDRIVE1OUT	Output	Pad	Drive 1 PWM output to control an external power transistor in a DC-DC converter circuit, with a software-programmable frequency and duty cycle.
DCDCDRIVEOE	Output	Pad	A common, active HIGH, output enable to control the bidirectional input/output pads fed by the drive 0 and drive 1 outputs, **DCDCDRIVE0OUT**, and **DCDCDRIVE1OUT**.

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