Cortex™-A7 NEON™ Media Processing Engine
Revision: r0p5
Cortex-A7 NEON Media Processing Engine

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Release Information

The following changes have been made to this book.

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
<th>Confidentiality</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 September 2011</td>
<td>A</td>
<td>Non-Confidential</td>
<td>First release for r0p0</td>
</tr>
<tr>
<td>08 November 2011</td>
<td>B</td>
<td>Non-Confidential</td>
<td>First release for r0p1</td>
</tr>
<tr>
<td>11 January 2012</td>
<td>C</td>
<td>Non-Confidential</td>
<td>First release for r0p2</td>
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<tr>
<td>03 May 2012</td>
<td>D</td>
<td>Non-Confidential</td>
<td>First release for r0p3</td>
</tr>
<tr>
<td>02 October 2012</td>
<td>E</td>
<td>Non-Confidential</td>
<td>First release for r0p4</td>
</tr>
<tr>
<td>10 April 2013</td>
<td>F</td>
<td>Confidential-Draft</td>
<td>First release for r0p5</td>
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</table>

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Product Status

The information in this document is final, that is for a developed product.

Web Address

http://www.arm.com
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Cortex-A7 NEON Media Processing Engine

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Preface

This preface introduces the *Cortex-A7 NEON Media Processing Engine Technical Reference Manual*. It contains the following sections:

- *About this book* on page v.
- *Feedback* on page viii.
About this book

This book is for the Cortex-A7 NEON Media Processing Engine (MPE). The book describes the external functionality of the Cortex-A7 NEON MPE.

Product revision status

The \textit{rpn} identifier indicates the revision status of the product described in this book, where:

- \textit{rn} Identifies the major revision of the product.
- \textit{pn} Identifies the minor revision or modification status of the product.

Intended audience

This book is written for system designers, system integrators, and programmers who are designing a System-on-Chip (SoC) that uses the Cortex-A7 NEON MPE.

Using this book

This book is organized into the following chapters:

- \textbf{Chapter 1 Introduction}
  
  Read this for a high-level view of the Cortex-A7 NEON MPE and a description of its features.

- \textbf{Chapter 2 Programmers Model}
  
  Read this for a description of the Cortex-A7 NEON MPE system registers.

- \textbf{Appendix A Revisions}
  
  Read this for a description of the technical changes between released issues of this book.

Glossary

The \textit{ARM Glossary} is a list of terms used in ARM documentation, together with definitions for those terms. The \textit{ARM Glossary} does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See ARM Glossary, \url{http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html}.

Conventions

Conventions that this book can use are described in:

- \textit{Typographical conventions on page vi}.
- \textit{Signals on page vi}.
Typographical conventions

The following table describes the typographical conventions:

<table>
<thead>
<tr>
<th>Style</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>italic</td>
<td>Introduces special terminology, denotes cross-references, and citations.</td>
</tr>
<tr>
<td>bold</td>
<td>Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.</td>
</tr>
<tr>
<td>monospace</td>
<td>Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.</td>
</tr>
<tr>
<td>monospace</td>
<td>Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.</td>
</tr>
<tr>
<td>monospace italic</td>
<td>Denotes arguments to monospace text where the argument is to be replaced by a specific value.</td>
</tr>
<tr>
<td>monospace bold</td>
<td>Denotes language keywords when used outside example code.</td>
</tr>
<tr>
<td>&lt;and&gt;</td>
<td>Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: MRC p15, o &lt;Rd&gt;, &lt;CRn&gt;, &lt;CRm&gt;, &lt;Opcode_2&gt;</td>
</tr>
<tr>
<td>SMALL CAPITALS</td>
<td>Used in body text for a few terms that have specific technical meanings, that are defined in the ARM glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.</td>
</tr>
</tbody>
</table>

Signals

The signal conventions are:

**Signal level**

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

**Lower-case n**

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter, [http://infocenter.arm.com](http://infocenter.arm.com), for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

The following confidential books are only available to licensees:

- CoreSight ETM-A7 Configuration and Sign-off Guide (ARM DII 0026).
- Cortex-A7 MPCore Configuration and Sign-off Guide (ARM DDI 0256).
- Cortex-A7 MPCore Integration Manual (ARM DIT 0017).

**Other publications**

This section lists relevant documents published by third parties:

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

• The product name.
• The product revision or version.
• An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

• The title.
• The number, ARM DDI 0462F.
• The page numbers to which your comments apply.
• A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter introduces the Cortex-A7 implementation of the ARM Single Instruction Multiple Data (SIMD) media processing architecture. It contains the following sections:

- About the Cortex-A7 NEON MPE on page 1-2.
- Applications on page 1-4.
- Product revisions on page 1-5.
1.1 About the Cortex-A7 NEON MPE

The Cortex-A7 NEON MPE extends the Cortex-A7 functionality to provide support for the ARMv7 Advanced SIMDv2 and Vector Floating-Pointv4 (VFPv4) instruction sets. The Cortex-A7 NEON MPE supports all addressing modes and data-processing operations described in the ARM Architecture Reference Manual.

The Cortex-A7 NEON MPE includes the following features:

• SIMD and scalar single-precision floating-point computation.
• Scalar double-precision floating-point computation.
• SIMD and scalar half-precision floating-point conversion.
• SIMD 8, 16, 32, and 64-bit signed and unsigned integer computation.
• 8 or 16-bit polynomial computation for single-bit coefficients.
• Structured data load capabilities.
• Large, shared register file, addressable as:
  — Thirty-two 32-bit S (single) registers.
  — Thirty-two 64-bit D (double) registers.
  — Sixteen 128-bit Q (quad) registers.

See the ARM Architecture Reference Manual for more information about the extension register set.

The operations include:

• Addition and subtraction.
• Multiplication with optional accumulation.
• Maximum or minimum value driven lane selection operations.
• Inverse square-root approximation.
• Comprehensive data-structure load instructions, including register-bank-resident table lookup.

1.1.1 VFPv4 architecture hardware support

The Cortex-A7 NEON MPE hardware supports single and double-precision add, subtract, multiply, divide, multiply and accumulate, fused multiply accumulate, and square root operations as described in the ARM VFPv4 architecture. It provides conversions between 16-bit, 32-bit, and 64-bit floating-point formats and ARM integer word formats, with special operations to perform conversions in round-towards-zero mode for high-level language support.

All instructions are available in both the ARM and Thumb instruction sets supported by the Cortex-A7 processor.

ARMv7 deprecates the use of VFP vector mode. The Cortex-A7 NEON MPE hardware does not support VFP vector operations. In this manual, the term vector refers to Advanced SIMD integer, polynomial and single-precision vector operations. The Cortex-A7 NEON MPE provides high speed VFP operation without support code. However, if an application requires VFP vector operation, then it must use support code. See the ARM Architecture Reference Manual for information on VFP vector operation support.
Note

This manual gives information specific to the Cortex-A7 NEON MPE implementation of the ARM Advanced SIMDv2 and VFPv4 extensions. See the *ARM Architecture Reference Manual* for full instruction set and usage details.
1.2 Applications

The Cortex-A7 NEON MPE provides mixed-data type SIMD and high-performance scalar floating-point computation suitable for a wide spectrum of applications such as:

- Personal digital assistants and smartphones for graphics, voice compression and decompression, user interfaces, Java interpretation, and Just In Time (JIT) compilation.
- Games machines for intensive three-dimensional graphics, digital audio and in-game physics effects such as gravity.
- Printers and MultiFunction Peripheral (MFP) controllers for high-definition color rendering.
- Set-top boxes for high-end digital audio and digital video, and interactive three-dimensional user interfaces.
- Automotive applications for engine management, power train computation, and in-car entertainment and navigation.
1.3 Product revisions

This section describes the differences in functionality between product revisions:

r0p0-r0p1 Functional changes are:
  • ID register value changed to reflect product revision status:
    FPSID Register 0x41023071.
    —— Note ——
    Product revision updated to maintain consistency with the main Cortex-A7 MPCore product.

r0p1-r0p2 Functional changes are:
  • ID register value changed to reflect product revision status:
    FPSID Register 0x41023072.
    —— Note ——
    Product revision updated to maintain consistency with the main Cortex-A7 MPCore product.

r0p2-r0p3 Functional changes are:
  • ID register value changed to reflect product revision status:
    FPSID Register 0x41023073.
    —— Note ——
    Product revision updated to maintain consistency with the main Cortex-A7 MPCore product.

r0p3-r0p4 Functional changes are:
  • ID register value changed to reflect product revision status:
    FPSID Register 0x41023074.
    —— Note ——
    Product revision updated to maintain consistency with the main Cortex-A7 MPCore product.

r0p4-r0p5 Functional changes are:
  • ID register value changed to reflect product revision status:
    FPSID Register 0x41023075.
    —— Note ——
    Product revision updated to maintain consistency with the main Cortex-A7 MPCore product.
Chapter 2
Programmers Model

This chapter describes the Cortex-A7 NEON MPE programmers model. It contains the following sections:

- About the programmers model on page 2-2.
- Advanced SIMD and VFP register access on page 2-4.
- Register summary on page 2-5.
- Register descriptions on page 2-6.
2.1 About the programmers model

This section introduces the Cortex-A7 NEON MPE implementation of the VFPv4 floating-point architecture, with version 2 of the Common VFP subarchitecture. In this implementation:

- All scalar operations are implemented entirely in hardware, with support for all combinations of rounding modes, flush-to-zero, and default NaN modes.
- Vector operations are not supported. Any attempt to execute a vector operation results in an Undefined Instruction exception with the FPEXC.DEX bit set to 1.
- The Cortex-A7 NEON MPE does not generate asynchronous VFP exceptions.

This section also provides information on initializing the Cortex-A7 NEON MPE ready for application code execution.

Table 2-2 on page 2-5 describes the following access types:

<table>
<thead>
<tr>
<th>Access Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>Read and write.</td>
</tr>
<tr>
<td>RO</td>
<td>Read only.</td>
</tr>
</tbody>
</table>

2.1.1 Accessing the Advanced SIMD and VFP feature identification registers

The Cortex-A7 NEON MPE implements the ARMv7 Advanced SIMD and VFP extensions. Software can identify these extensions and the features they provide, using the feature identification registers. These registers reside in the coprocessor space for coprocessors CP10 and CP11. You can access the registers using the VMRS and VMSR instructions, for example:

```asm
VMRS <Rd>, FPSID ; Read Floating-Point System ID Register
VMRS <Rd>, MVFR1 ; Read Media and VFP Feature Register 1
VMSR FPSCR, <Rt> ; Write Floating-Point System Control Register
```

See Register descriptions on page 2-6 for a description of the registers.

2.1.2 Enabling Advanced SIMD and VFP support

From reset, both the Advanced SIMD and VFP extensions are disabled. Any attempt to execute either an Advanced SIMD or VFP instruction results in an Undefined Instruction exception being taken. To enable software to access Advanced SIMD and VFP features ensure that:

- Access to CP10 and CP11 is enabled for the appropriate privilege level. See Advanced SIMD and VFP register access on page 2-4.
- If Non-secure access to the Advanced SIMD features or VFP features is required, the access flags for CP10 and CP11 in the NSACR must be set to 1. See Advanced SIMD and VFP register access on page 2-4.

In addition, software must set the FPEXC.EN bit to 1 to enable most Advanced SIMD and VFP operations. See Floating-Point Exception Register on page 2-10.

When Advanced SIMD and VFP operation is disabled because FPEXC.EN is 0, all Advanced SIMD and VFP instructions are treated as UNDEFINED instructions except for execution of the following in privileged modes:

- A VMRS to the FPEXC or FPSID register.
- A VMRS from the FPEXC, FPSID, MVFR0, or MVFR1 registers.
To use the NEON MPE in Secure state only

To use the NEON MPE in Secure state only, define the CPACR and Floating-Point Exception (FPEXC) registers to enable the NEON MPE:

1. Set the CPACR for access to CP10 and CP11, and clear the ASEDIS and D32DIS bits:
   \[
   \text{LDR } r0, = (0xF << 20) \\
   \text{MCR } p15, 0, r0, c1, c0, 2
   \]

2. Set the FPEXC EN bit to enable the NEON MPE:
   \[
   \text{MOV } r3, #0x40000000 \\
   \text{VMSR } \text{FPEXC}, r3
   \]

At this point the Cortex-A7 processor can execute Advanced SIMD and VFP instructions.

To use the NEON MPE in Secure state and Non-secure state

To use the NEON MPE in Secure state and Non-secure state, first define the NSACR and then define the CPACR and FPEXC registers to enable the NEON MPE.

1. Set bits [11:10] of the NSACR for access to CP10 and CP11 from both Secure and Non-secure states, and clear the NSASEDIS and NSD32DIS bits:
   \[
   \text{MRC } p15, 0, r0, c1, c1, 2 \\
   \text{ORR } r0, r0, 2_11<<10 \ ; \text{ enable neon} \\
   \text{BIC } r0, r0, 2_11<<14 \ ; \text{ clear nsasedis/nsd32dis} \\
   \text{MCR } p15, 0, r0, c1, c1, 2
   \]

2. Set the CPACR for access to CP10 and CP11, and clear the ASEDIS and D32DIS bits:
   \[
   \text{LDR } r0, = (0xF << 20) \\
   \text{MCR } p15, 0, r0, c1, c0, 2
   \]

3. Set the FPEXC EN bit to enable the NEON MPE:
   \[
   \text{MOV } r3, #0x40000000 \\
   \text{VMSR } \text{FPEXC}, r3
   \]

At this point the Cortex-A7 processor can execute Advanced SIMD and VFP instructions.

--- Note ---

Operation is UNPREDICTABLE if you configure the Coprocessor Access Control Register (CPACR) such that CP10 and CP11 do not have identical access permissions.
2.2 Advanced SIMD and VFP register access

Table 2-1 shows the system control coprocessor registers, accessed through CP15, that determine access to Advanced SIMD and VFP registers, where:

- CRn is the register number within CP15.
- Op1 is the Opcode_1 value for the register.
- CRm is the operational register.
- Op2 is the Opcode_2 value for the register.

<table>
<thead>
<tr>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c1</td>
<td>0</td>
<td>c0</td>
<td>2</td>
<td>CPACR</td>
<td>See the Cortex-A7 MPCore Technical Reference Manual</td>
</tr>
<tr>
<td>c1</td>
<td>0</td>
<td>c1</td>
<td>2</td>
<td>NSACR</td>
<td>See the Cortex-A7 MPCore Technical Reference Manual</td>
</tr>
</tbody>
</table>
2.3 Register summary

Table 2-2 shows the Cortex-A7 NEON MPE system registers. All NEON MPE system registers are 32-bit wide. Reserved register addresses are UNPREDICTABLE.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPSID</td>
<td>RO</td>
<td>0x41023075</td>
<td>Floating-Point System ID Register on page 2-6</td>
</tr>
<tr>
<td>FPSCR</td>
<td>RW</td>
<td>0x00000000</td>
<td>Floating-Point Status and Control Register on page 2-7</td>
</tr>
<tr>
<td>MVFR0</td>
<td>RO</td>
<td>0x10110222</td>
<td>Media and VFP Feature Register 0 on page 2-8</td>
</tr>
<tr>
<td>MVFR1</td>
<td>RO</td>
<td>0x11111111</td>
<td>Media and VFP Feature Register 1 on page 2-9</td>
</tr>
<tr>
<td>FPEXC</td>
<td>RW</td>
<td>0x00000000</td>
<td>Floating-Point Exception Register on page 2-10</td>
</tr>
</tbody>
</table>

**Note**
The FPINST and FPINST2 registers are not implemented, and any attempt to access them is UNPREDICTABLE.

Table 2-3 shows the processor modes for accessing the Cortex-A7 NEON MPE system registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Privileged access</th>
<th>User access</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FPEXC EN=0</td>
<td>FPEXC EN=1</td>
</tr>
<tr>
<td>FPSID</td>
<td>Permitted</td>
<td>Permitted</td>
</tr>
<tr>
<td>FPSCR</td>
<td>Not permitted</td>
<td>Permitted</td>
</tr>
<tr>
<td>MVFR0, MVFR1</td>
<td>Permitted</td>
<td>Permitted</td>
</tr>
<tr>
<td>FPEXC</td>
<td>Permitted</td>
<td>Permitted</td>
</tr>
</tbody>
</table>
2.4 Register descriptions

This section describes the Cortex-A7 NEON MPE system registers. Table 2-2 on page 2-5 provides cross references to individual registers.

2.4.1 Floating-Point System ID Register

The FPSID characteristics are:

**Purpose**
Provides information about the VFP implementation.

**Usage constraints**
This register is:
- Only accessible in the Non-secure state if the CP10 and CP11 bits in the NSACR are set to 1, see Advanced SIMD and VFP register access on page 2-4.
- Only accessible in privileged modes, and only if access to coprocessors CP10 and CP11 is enabled in the CPACR and FPEXC.EN is set to 1, see Advanced SIMD and VFP register access on page 2-4.

**Configurations**
Available in all configurations.

**Attributes**
See the register summary in Table 2-2 on page 2-5.

Figure 2-1 shows the FPSID bit assignments.

![Figure 2-1 FPSID bit assignments](image)

Table 2-4 shows the FPSID bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:24]</td>
<td>Implementer</td>
<td>Denotes ARM. Value is 0x41.</td>
</tr>
<tr>
<td>[23]</td>
<td>SW</td>
<td>Hardware implementation with no software emulation. Value is 0x0.</td>
</tr>
<tr>
<td>[22:16]</td>
<td>Subarchitecture</td>
<td>VFPv3 or greater with v2 subarchitecture. Value is 0x2.</td>
</tr>
<tr>
<td>[15:8]</td>
<td>Part number</td>
<td>Cortex-A. Value is 0x30.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>Revision</td>
<td>Revision. Value is 0x5.</td>
</tr>
</tbody>
</table>

You can access the FPSID Register with the following VMRS instruction:

VMRS <Rd>, FPSID ; Read Floating-Point System ID Register
### 2.4.2 Floating-Point Status and Control Register

The FPSCR characteristics are:

**Purpose**

Provides User level control of the NEON MPE.

**Usage constraints**

This register is:

- Only accessible in the Non-secure state if the CP10 and CP11 bits in the NSACR are set to 1, see *Advanced SIMD and VFP register access* on page 2-4.
- Accessible in all modes depending on the setting of bits [23:20] of the CPACR and FPEXC.EN, see *Advanced SIMD and VFP register access* on page 2-4.

**Configurations**

Available in all configurations.

**Attributes**

See the register summary in Table 2-2 on page 2-5.

Figure 2-2 shows the FPSCR bit summary in Table 2-2 on page 2-5.

![Figure 2-2 FPSCR bit assignments](image)

Table 2-5 shows the FPSCR bit assignments.

![Table 2-5 FPSCR bit assignments](image)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>N</td>
<td>Set to 1 if a comparison operation produces a less than result.</td>
</tr>
<tr>
<td>[30]</td>
<td>Z</td>
<td>Set to 1 if a comparison operation produces an equal result.</td>
</tr>
<tr>
<td>[29]</td>
<td>C</td>
<td>Set to 1 if a comparison operation produces an equal, greater than, or unordered result.</td>
</tr>
<tr>
<td>[28]</td>
<td>V</td>
<td>Set to 1 if a comparison operation produces an unordered result.</td>
</tr>
<tr>
<td>[27]</td>
<td>QC</td>
<td>Set to 1 if an Advanced SIMD integer operation has saturated since 0 was last written to this bit.</td>
</tr>
<tr>
<td>[26]</td>
<td>AHP</td>
<td>Alternative Half-Precision control bit:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 IEEE half-precision format selected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Alternative half-precision format selected.</td>
</tr>
<tr>
<td>[25]</td>
<td>DN</td>
<td>Default NaN mode control bit:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 NaN operands propagate through to the output of a floating-point operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Any operation involving one or more NaNs returns the Default NaN.</td>
</tr>
</tbody>
</table>

Advanced SIMD arithmetic always uses the Default NaN setting, regardless of the value of the DN bit.
You can access the FPSCR with the following VMRS and VMSR instructions:

VMRS <Rd>, FPSCR ; Read Floating-Point Status and Control Register
VMSR FPSCR, <Rt> ; Write Floating-Point Status and Control Register

### 2.4.3 Media and VFP Feature Register 0

The MVFR0 characteristics are:

**Purpose**

Together with MVFR1, describes the features that the NEON MPE provides.

**Usage constraints**

This register is:

- Only accessible in the Non-secure state if the CP10 and CP11 bits in the NSACR are set to 1, see *Advanced SIMD and VFP register access on page 2-4*. 

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[24]</td>
<td>FZ</td>
<td>Flush-to-zero mode control bit:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Flush-to-zero mode disabled. Behavior of the floating-point system is fully compliant with the IEEE 754 standard.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Flush-to-zero mode enabled. Advanced SIMD arithmetic always uses the Flush-to-zero setting, regardless of the value of the FZ bit.</td>
</tr>
<tr>
<td>[23:22]</td>
<td>RMode</td>
<td>Rounding Mode control field:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>b00 \textit{Round to Nearest} (RN) mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>b01 \textit{Round towards Plus infinity} (RP) mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>b10 \textit{Round towards Minus infinity} (RM) mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>b11 \textit{Round towards Zero} (RZ) mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Advanced SIMD arithmetic always uses the Round to Nearest setting, regardless of the value of the RMode bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The Cortex-A7 NEON MPE ignores the value of this field.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See the <em>ARM Architecture Reference Manual</em>.</td>
</tr>
<tr>
<td>[19]</td>
<td>Reserved</td>
<td>UNK/SBZP.</td>
</tr>
<tr>
<td>[18:16]</td>
<td>Len</td>
<td>Vector length, used for backwards compatibility with short vector operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If you set this field to a non-zero value, the VFP data-processing instructions generate exceptions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See the <em>ARM Architecture Reference Manual</em>.</td>
</tr>
<tr>
<td>[15:8]</td>
<td>Reserved</td>
<td>UNK/SBZP.</td>
</tr>
<tr>
<td>[6:5]</td>
<td>Reserved</td>
<td>UNK/SBZP.</td>
</tr>
<tr>
<td>[1]</td>
<td>DZC</td>
<td>Division by Zero cumulative exception flag.</td>
</tr>
<tr>
<td>[0]</td>
<td>IOC</td>
<td>Invalid Operation cumulative exception flag.</td>
</tr>
</tbody>
</table>
• Only accessible in privileged modes, and only if access to coprocessors CP10 and CP11 is enabled in the CPACR and FPEXC.EN is set to 1, see Advanced SIMD and VFP register access on page 2-4.

Configurations Available in all configurations.

Attributes See the register summary in Table 2-2 on page 2-5.

Figure 2-3 shows the MVFR0 bit assignments.

Table 2-6 shows the MVFR0 bit assignments.

Table 2-6 MVFR0 bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:28]</td>
<td>VFP rounding modes</td>
<td>All rounding modes supported. Value is 0x1.</td>
</tr>
<tr>
<td>[27:24]</td>
<td>Short vectors</td>
<td>Short vectors not supported. Value is 0x0.</td>
</tr>
<tr>
<td>[23:20]</td>
<td>Square root</td>
<td>Hardware square root supported. Value is 0x1.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>Divide</td>
<td>Hardware divide supported. Value is 0x1.</td>
</tr>
<tr>
<td>[15:12]</td>
<td>VFP exception trapping</td>
<td>Software traps not supported. Value is 0x0.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>A_SIMD registers</td>
<td>Thirty-two 64-bit registers supported. Value is 0x2.</td>
</tr>
</tbody>
</table>

You can access the MVFR0 with the following VMRS instruction:

VMRS <Rd>, MVFR0 ; Read Media and VFP Feature Register 0

2.4.4 Media and VFP Feature Register 1

The MVFR1 characteristics are:

Purpose Together with MVFR0, describes the features that the NEON MPE provides.

Usage constraints This register is:

• Only accessible in the Non-secure state if the CP10 and CP11 bits in the NSACR are set to 1, see Advanced SIMD and VFP register access on page 2-4.

• Only accessible in privileged modes, and only if access to coprocessors CP10 and CP11 is enabled in the CPACR and FPEXC.EN is set to 1, see Advanced SIMD and VFP register access on page 2-4.

Configurations Available in all configurations.
Attributes See the register summary in Table 2-2 on page 2-5.

Figure 2-4 shows the MVFR1 bit assignments.

Table 2-7 shows the MVFR1 bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:28]</td>
<td>A_SIMD FMAC</td>
<td>Fused Multiply Accumulate supported. Value is 0x1.</td>
</tr>
<tr>
<td>[27:24]</td>
<td>VFP HPFP</td>
<td>VFP half-precision operations supported. Value is 0x1.</td>
</tr>
<tr>
<td>[23:20]</td>
<td>A_SIMD HPFP</td>
<td>Advanced SIMD half-precision operations supported. Value is 0x1.</td>
</tr>
<tr>
<td>[15:12]</td>
<td>A_SIMD integer</td>
<td>Advanced SIMD integer operations supported. Value is 0x1.</td>
</tr>
<tr>
<td>[7:4]</td>
<td>D_NaN mode</td>
<td>Propagation of NaN values supported for VFP. Value is 0x1.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>FZ</td>
<td>Full denormal arithmetic operations supported for VFP. Value is 0x1.</td>
</tr>
</tbody>
</table>

You can access the MVFR1 with the following VMRS instruction:

VMRS <Rd>, MVFR1 ; Read Media and VFP Feature Register 1

2.4.5 Floating-Point Exception Register

The FPEXC characteristics are:

Purpose Provides global enable control of the Advanced SIMD and VFP extensions.

Usage constraints This register is:

- Only accessible in the Non-secure state if the CP10 and CP11 bits in the NSACR are set to 1, see Advanced SIMD and VFP register access on page 2-4.
- Only accessible in privileged modes, and only if access to coprocessors CP10 and CP11 is enabled in the CPACR, see Advanced SIMD and VFP register access on page 2-4.

Configurations Available in all configurations.

Attributes See the register summary in Table 2-2 on page 2-5.

Figure 2-5 on page 2-11 shows the FPEXC bit assignments.
Table 2-8 shows the FPEXC bit assignments.

Table 2-8 FPEXC bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>EX</td>
<td>The Cortex-A7 NEON MPE does not generate asynchronous VFP exceptions, therefore this bit is RAZ/WI.</td>
</tr>
</tbody>
</table>
| [30] | EN   | NEON MPE enable bit:  
0  NEON MPE disabled.  
1  NEON MPE enabled.  
The EN bit is cleared to 0 at reset. |
| [29] | DEX  | Defined synchronous instruction exceptional flag. The Cortex-A7 NEON MPE sets this bit to 1 when generating a synchronous bounce because of an attempt to execute a vector operation. All other Undefined Instruction exceptions clear this bit to zero.  
See the ARM Architecture Reference Manual for more information. |
| [28:0] | Reserved | RAZ/WI. |

Note

The Cortex-A7 NEON MPE hardware does not support the deprecated VFP short vector feature. Attempts to execute VFP data-processing instructions when the FPSCR.LEN field is non-zero set the FPSCR.DEX bit and result in a synchronous VFP Exception. You can use software to emulate the short vector feature, if required.

You can access the FPEXC Register with the following VMRS and VMSR instructions:

VMRS <Rd>, FPEXC  ; Read Floating-Point Exception Register  
VMSR FPEXC, <Rt>  ; Write Floating-Point Exception Register
## Appendix A
### Revisions

This appendix describes the technical changes between released issues of this book.

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>No changes, first release</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Table A-2 Differences between issue A and issue B**

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated reset value of the FPSID Register</td>
<td>Table 2-2 on page 2-5</td>
<td>r0p1</td>
</tr>
<tr>
<td>Updated bits[3:0] of the FPSID Register</td>
<td>Table 2-4 on page 2-6</td>
<td>r0p1</td>
</tr>
</tbody>
</table>

**Table A-3 Differences between issue B and issue C**

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated reset value of the FPSID Register</td>
<td>Table 2-2 on page 2-5</td>
<td>r0p2</td>
</tr>
<tr>
<td>Updated bits[3:0] of the FPSID Register</td>
<td>Table 2-4 on page 2-6</td>
<td>r0p2</td>
</tr>
</tbody>
</table>
### Table A-4 Differences between issue C and issue D

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated reset value of the FPSID Register</td>
<td>Table 2-2 on page 2-5</td>
<td>r0p3</td>
</tr>
<tr>
<td>Updated bits[3:0] of the FPSID Register</td>
<td>Table 2-4 on page 2-6</td>
<td>r0p3</td>
</tr>
</tbody>
</table>

### Table A-5 Differences between issue D and issue E

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated reset value of the FPSID Register</td>
<td>Table 2-2 on page 2-5</td>
<td>r0p4</td>
</tr>
<tr>
<td>Updated bits[3:0] of the FPSID Register</td>
<td>Table 2-4 on page 2-6</td>
<td>r0p4</td>
</tr>
</tbody>
</table>

### Table A-6 Differences between issue E and issue F

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated reset value of the FPSID Register</td>
<td>Table 2-2 on page 2-5</td>
<td>r0p5</td>
</tr>
<tr>
<td>Updated bits[3:0] of the FPSID Register</td>
<td>Table 2-4 on page 2-6</td>
<td>r0p5</td>
</tr>
</tbody>
</table>