Release Information

The following changes have been made to this book.

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
<th>Confidentiality</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>09 August 2013</td>
<td>A</td>
<td>Confidential</td>
<td>Release for r0p0</td>
</tr>
<tr>
<td>04 November 2013</td>
<td>B</td>
<td>Confidential</td>
<td>Release for r0p1</td>
</tr>
<tr>
<td>13 December 2013</td>
<td>C</td>
<td>Confidential</td>
<td>Release for r0p2</td>
</tr>
<tr>
<td>30 April 2014</td>
<td>D</td>
<td>Confidential</td>
<td>Release for r0p3</td>
</tr>
<tr>
<td>29 July 2014</td>
<td>E</td>
<td>Confidential</td>
<td>Release for r0p4</td>
</tr>
<tr>
<td>16 December 2015</td>
<td>F</td>
<td>Non-Confidential</td>
<td>Second release for r0p4</td>
</tr>
</tbody>
</table>

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Product Status

The information in this document is final, that is for a developed product.

Web Address

http://www.arm.com
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Appendix A Revisions
Preface

This preface introduces the ARM® Cortex®-A53 MPCore Cryptography Extension Technical Reference Manual. It contains the following sections:

• *About this book* on page v.
• *Feedback* on page vii.
About this book

This book is for the Cortex-A53 MPCore Cryptography Extension.

Product revision status

The rmpn identifier indicates the revision status of the product described in this book, for example, r1p2, where:

- **rm** Identifies the major revision of the product, for example, r1.
- **pn** Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses the Cortex-A53 processor with the optional Cryptography Extension.

Using this book

This book is organized into the following chapters:

- **Chapter 1 Introduction**
  Read this for an introduction to the Cortex-A53 processor Cryptography Extension.

- **Chapter 2 Programmers Model**
  Read this for a description of the Cortex-A53 processor Cryptography Extension programmers model.

- **Appendix A Revisions**
  Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM® Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM® Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.


Conventions

This book uses the conventions that are described in:

- *Typographical conventions on page vi.*
Typographical conventions

The following table describes the typographical conventions:

<table>
<thead>
<tr>
<th>Style</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>italic</td>
<td>Introduces special terminology, denotes cross-references, and citations.</td>
</tr>
<tr>
<td>bold</td>
<td>Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.</td>
</tr>
<tr>
<td>monospace</td>
<td>Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.</td>
</tr>
<tr>
<td>monospace bold</td>
<td>Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.</td>
</tr>
<tr>
<td>monospace italic</td>
<td>Denotes arguments to monospace text where the argument is to be replaced by a specific value.</td>
</tr>
<tr>
<td>looks</td>
<td>Denotes language keywords when used outside example code.</td>
</tr>
<tr>
<td>&lt;and&gt;</td>
<td>Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: MRC p15, 0 &lt;Rd&gt;, &lt;CRn&gt;, &lt;CRm&gt;, &lt;0pcode_2&gt;</td>
</tr>
</tbody>
</table>

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter [http://infocenter.arm.com](http://infocenter.arm.com), for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:


Other publications

This section lists relevant documents published by third parties:

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

• The product name.
• The product revision or version.
• An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:

• The title.
• The number, ARM DDI 0501F.
• The page numbers to which your comments apply.
• A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Note

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Chapter 1
Introduction

This chapter describes the Cortex-A53 MPCore Cryptography Extension. It contains the following sections:

- About the Cortex-A53 processor Cryptography Extension on page 1-2.
- Revisions on page 1-3.
1.1 About the Cortex-A53 processor Cryptography Extension


Note

The optional Cryptography Extension is not included in the base product. ARM supplies the Cryptography Extension only under an additional licence to the Cortex-A53 processor and Advanced SIMD and Floating-point support licences.
1.2 Revisions

This section describes the differences in functionality between product revisions:

- **r0p0**: First release.
- **r0p1**: There are no functional changes in this revision.
- **r0p2**: There are no functional changes in this revision.
- **r0p3**: There are no functional changes in this revision.
- **r0p4**: There are no functional changes in this revision.
Chapter 2
Programmers Model

This chapter describes the programmers model. It contains the following sections:

- About the programmers model on page 2-2.
- Register summary on page 2-3.
- Register descriptions on page 2-4.
2.1 About the programmers model

This section describes the registers of the Cortex-A53 processor Cryptography Extension and provides programming information. See the *ARM® Architecture Reference Manual, ARMv8* for more information.

This section describes:
- Identifying the cryptography instructions implemented.
- Disabling the Cryptography Extension.

2.1.1 Identifying the cryptography instructions implemented

Software can identify the cryptography instructions implemented by reading:
- ID_AA64ISAR0_EL1 in the AArch64 execution state.
- ID_ISAR5_EL1 in the AArch64 execution state.
- ID_ISAR5 in the AArch32 execution state.

2.1.2 Disabling the Cryptography Extension

To disable the Cryptography Extension for each individual core, assert the corresponding bit of the CRYPTODISABLE input signal. This signal is only sampled during reset of the core.

When CRYPTODISABLE is asserted:
- Executing a cryptography instruction results in an UNDEFINED exception.
- The ID registers described in Table 2-1 on page 2-3 indicate that the Cryptography Extension is not implemented.
2.2 Register summary

Table 2-1 lists the instruction identification registers for the Cortex-A53 processor Cryptography Extension.

Table 2-1 Cryptography extension register summary

<table>
<thead>
<tr>
<th>Name</th>
<th>Execution state</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID_AA64ISAR0_EL1</td>
<td>AArch64</td>
<td>See <em>AArch64 Instruction Set Attribute Register 0, EL1</em> on page 2-4.</td>
</tr>
<tr>
<td>ID_ISAR5</td>
<td>AArch32</td>
<td>See <em>Instruction Set Attribute Register 5</em> on page 2-6.</td>
</tr>
<tr>
<td>ID_ISAR5_EL1</td>
<td>AArch64</td>
<td>See <em>Instruction Set Attribute Register 5</em> on page 2-6.</td>
</tr>
</tbody>
</table>
2.3 Register descriptions

This section describes the Cortex-A53 processor Cryptography Extension registers. Table 2-1 on page 2-3 provides cross references to individual registers.

2.3.1 AArch64 Instruction Set Attribute Register 0, EL1

The ID-AA64ISAR0_EL1 characteristics are:

**Purpose**: Provides information about the optional cryptography instructions that the processor can support.

**Usage constraints**: This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**: ID-AA64ISAR0_EL1 is architecturally mapped to external register ID-AA64ISAR0.

**Attributes**: ID-AA64ISAR0_EL1 is a 64-bit register.

Figure 2-1 shows the ID-AA64ISAR0_EL1 bit assignments.

![Figure 2-1 ID-AA64ISAR0_EL1 bit assignments](image)

Table 2-2 shows the ID-AA64ISAR0_EL1 bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:20]</td>
<td>-</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>CRC32</td>
<td>CRC32 instructions are implemented.</td>
</tr>
<tr>
<td>[15:12]</td>
<td>SHA2</td>
<td>Indicates whether SHA2 instructions are implemented. The possible values are:</td>
</tr>
<tr>
<td></td>
<td>0x0</td>
<td>No SHA2 instructions are implemented. This is the value if the implementation does not include the Cryptography Extension.</td>
</tr>
<tr>
<td></td>
<td>0x1</td>
<td>SHA256H, SHA256H2, SHA256U0, and SHA256U1 implemented. This is the value if the implementation includes the Cryptography Extension.</td>
</tr>
</tbody>
</table>
To access the ID_AA64ISAR0_EL1:

```assembly
MRS <Xt>, ID_AA64ISAR0_EL1 ; Read ID_AA64ISAR0_EL1 into Xt

ID_AA64ISAR0_EL1[31:0] can be accessed through the internal memory-mapped interface and the external debug interface, offset 0xD30.

Register access is encoded as follows:

### Table 2-3 ID_AA64ISAR0_EL1 access encoding

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>000</td>
<td>0000</td>
<td>0110</td>
<td>000</td>
</tr>
</tbody>
</table>

#### 2.3.2 AArch32 Instruction Set Attribute Register 5

The ID_ISAR5_EL1 characteristics are:

**Purpose**
Provides information about the instruction sets that the processor implements.

**Note**
The optional Cryptography Extension is not included in the base product of the processor. ARM requires licensees to have contractual rights to obtain the Cryptography Extension.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (ES)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**
ID_ISAR5_EL1 is architecturally mapped to AArch32 register ID_ISAR5. See Instruction Set Attribute Register 5 on page 2-6.

**Attributes**
ID_ISAR5_EL1 is a 32-bit register.

Figure 2-2 on page 2-6 shows the ID_ISAR5_EL1 bit assignments.
Table 2-4 shows the ID_ISAR5_EL1 bit assignments.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:20]</td>
<td>-</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>
| [19:16] | CRC32 | Indicates whether CRC32 instructions are implemented in AArch32 state. The value is:  
0x1 CRC32 instructions are implemented. |
| [15:12] | SHA2 | Indicates whether SHA2 instructions are implemented in AArch32 state. The possible values are:  
0x0 Cryptography Extensions are not implemented or are disabled.  
0x1 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions are implemented. |
| [11:8] | SHA1 | Indicates whether SHA1 instructions are implemented in AArch32 state. The possible values are:  
0x0 Cryptography Extensions are not implemented or are disabled.  
0x1 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions are implemented. |
| [7:4] | AES | Indicates whether AES instructions are implemented in AArch32 state. The possible values are:  
0x0 Cryptography Extensions are not implemented or are disabled.  
0x2 AESE, AESD, AESMC, and AESIMC are implemented, plus PMULL and PMULL2 instructions operating on 64-bit data. |
| [3:0] | SEVL | Indicates whether the SEVL instruction is implemented. The value is:  
0x1 SEVL implemented to send event local. |

To access the ID_ISAR5_EL1:

MRS <Xt>, ID_ISAR5_EL1 ; Read ID_ISAR5_EL1 into Xt

Register access is encoded as follows:

Table 2-5 ID_ISAR5_EL1 access encoding

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>000</td>
<td>0000</td>
<td>0010</td>
<td>101</td>
</tr>
</tbody>
</table>

### 2.3.3 Instruction Set Attribute Register 5

The ID_ISAR5 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the processor in AArch32.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>
The ID_ISAR5 must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, and ID_ISAR4.

**Configurations**

ID_ISAR5 is architecturally mapped to AArch64 register ID_ISAR5_EL1. See *AArch32 Instruction Set Attribute Register 5 on page 2-5*.

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

ID_ISAR5 is a 32-bit register.

Figure 2-3 shows the ID_ISAR5 bit assignments.

```
<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:20]</td>
<td>-</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>CRC32</td>
<td>Indicates whether CRC32 instructions are implemented in AArch32 state. The value is: 0x0 CRC32 instructions are not implemented. 0x1 CRC32 instructions are implemented.</td>
</tr>
<tr>
<td>[15:12]</td>
<td>SHA2</td>
<td>Indicates whether SHA2 instructions are implemented in AArch32 state. The possible values are: 0x0 Cryptographic extensions are not implemented or are disabled. 0x1 SHA256H, SHA256H2, SHA256S0, and SHA256SUL instructions are implemented.</td>
</tr>
<tr>
<td>[11:8]</td>
<td>SHA1</td>
<td>Indicates whether SHA1 instructions are implemented in AArch32 state. The possible values are: 0x0 Cryptographic extensions are not implemented or are disabled. 0x1 SHA1C, SHA1P, SHA1M, SHA1H, SHA1S0, and SHA1SUL instructions are implemented.</td>
</tr>
<tr>
<td>[7:4]</td>
<td>AES</td>
<td>Indicates whether AES instructions are implemented in AArch32 state. The possible values are: 0x0 Cryptographic extensions are not implemented or are disabled. 0x2 AESCE, AES0, AESMC and AESIMC, plus PMULL and PMULL2 instructions operating on 64-bit data.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>SEVL</td>
<td>Indicates whether the SEVL instruction is implemented. The value is: 0x0 SEVL implemented to send event local.</td>
</tr>
</tbody>
</table>
```

Table 2-6 shows the ID_ISAR5 bit assignments.

To access ID_ISAR5:

```
MRC p15, 0, <Rt>, c0, c2, s; Read ID_ISAR5 into Rt
```
Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

<table>
<thead>
<tr>
<th>Table A-1 Issue A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change</td>
</tr>
<tr>
<td>First revision</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table A-2 Differences between Issue A and Issue B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change</td>
</tr>
<tr>
<td>There are no technical changes between these released issues.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table A-3 Differences between Issue B and Issue C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change</td>
</tr>
<tr>
<td>There are no technical changes between these released issues.</td>
</tr>
</tbody>
</table>
### Table A-4 Differences between Issue C and Issue D

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>There are no technical changes between these released issues.</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Table A-5 Differences between Issue D and Issue E

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>There are no technical changes between these released issues.</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Table A-6 Differences between Issue E and Issue F

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Document confidentiality changed.</td>
<td>Throughout</td>
<td>Issue F</td>
</tr>
</tbody>
</table>