



# PrimeCell® Infrastructure AMBA™ 3 AXI™ Register Slice (BP130) Revision: r0p0 **Technical Overview**

This technical overview describes the functionality of the AXI register slice in the following sections:

- *Preliminary material* on page 2
- *About the AXI register slice* on page 4
- *Functional description* on page 5
- *Physical data* on page 8
- *Signal descriptions* on page 9.

# 1 Preliminary material

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## 1.1 Release information

Changes to this document are listed in Table 1.

**Table 1 Change history**

Date	Issue	Change
26 November 2004	A	First issue for r0p0

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## 1.4 Product status

The information in this document is for a final product, that is a developed product.

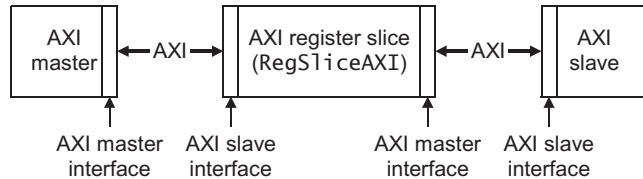
## 1.5 Web address

<http://www.arm.com>

## 2 About the AXI register slice

You can use the AXI register slice, `RegSliceAxi`, to register an AXI interconnect and provide timing isolation. The component is hierarchical and it is constructed of specific components for each AXI channel that enable you to register them individually.

Figure 1 shows the AXI register slice block diagram.



**Figure 1 AXI register slice block diagram**

The `RegSliceAxi` component has the following features:

- statically configurable data width of 64 bits or 32 bits
- statically configurable ID width
- statically configurable bus-width for the user and channel-specific sideband signals
- statically configurable register slice type to use for each AXI channel
- the HDL code is supplied as Verilog.

The interface does not have an AXI low-power interface because it does not initiate transactions or have a low-power mode of operation.

### 3 Functional description

The AXI register slice is described in:

- *Operating modes*
- *Interface attributes* on page 6.

#### 3.1 Operating modes

You can configure the RegSliceAXI to operate in one of three modes for each AXI channel as described in:

- *Fully registered*
- *Registered forward path*
- *Static bypass* on page 6.

##### Fully registered

This is the default configuration. It provides complete timing isolation between two points within an AXI interconnect. Figure 2 shows this.

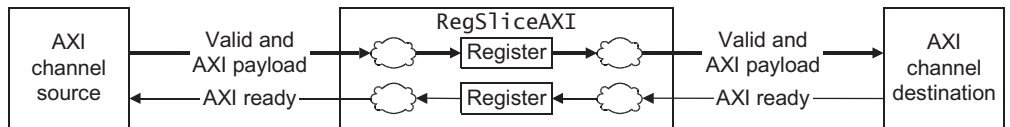


Figure 2 Fully registered configuration

##### Registered forward path

The valid and payload signals are isolated in this configuration. The ready signal for the channel source is a combinatorial path from the channel destination. Figure 3 shows this.

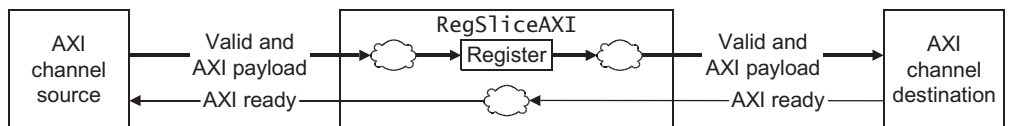


Figure 3 Registered forward path configuration

### Static bypass

No timing isolation is used in this configuration. The master and slave interfaces of the channel are directly connected. Figure 4 shows bypass mode.

You can include the register slice in a system design irrespective of requirement. If initial synthesis runs then show critical paths through the interconnect, you can switch the register slice out of bypass mode to solve the problem.

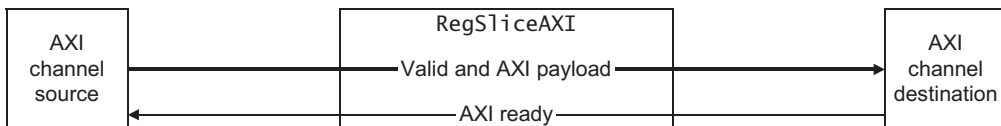


Figure 4 Static bypass configuration

### 3.2 Interface attributes

The master and slave interface attributes for the AXI register slice are described in:

- Table 2
- Table 3 on page 7.

Table 2 Master interface attributes

Attribute	Description	Value
Write ID capability	The maximum number of different <b>AWID</b> values that a master can generate for all active write transactions at any one time	Master-dependent
Write ID width	The number of bits in the <b>AWID</b> and <b>WID</b> buses.	Master-dependent
Write issuing capability	The maximum number of active write transactions that a master can generate.	Master-dependent
Read ID capability	The maximum number of different <b>ARID</b> values that a master can generate for all active read transactions at any one time.	Master-dependent
Read ID width	The number of bits in the <b>ARID</b> bus.	Master-dependent
Read issuing capability	The maximum number of active read transactions that a master can generate.	Master-dependent

**Table 3 Slave interface attributes**

<b>Attribute</b>	<b>Description</b>	<b>Value</b>
Write acceptance capability	The maximum number of active write transactions that a slave can accept.	Slave-dependent
Read acceptance capability	The maximum number of active read transactions that a slave can accept.	Slave-dependent
Write interleave depth	The number of active write transactions for which the slave can receive data. This is counted from the earliest transaction.	Slave-dependent
Read data reorder depth	The number of active read transactions for which a slave may transmit data. This is counted from the earliest transaction.	Slave-dependent

**Note**

Master-dependent and slave-dependent used in the Value column of Table 2 on page 6 and Table 3 mean that the register slice adopts the attribute value of the master or slave that the relevant interface is connected to.

## 4 Physical data

This section describes:

- *AC characteristics*
- *Gate count.*

### 4.1 AC characteristics

The AXI register slice adheres to the following timing guidelines. The figures refer to the percentage of clock cycle allowed for each function:

- inputs to registers must be valid for 40% of the cycle prior to the rising edge of the clock
- outputs from registers must be valid for 20% of the cycle after the rising edge of the clock
- forward path register mode combinatorial paths must not take longer than 5% of the complete clock cycle.

Timing characteristics are confirmed by performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process at a target speed of 200MHz.

### 4.2 Gate count

Table 4 lists the estimated total gate counts with respect to the library described in *AC characteristics*.

**Table 4 Gate count estimates**

<b>Variant</b>	<b>NAND2X1 equivalents</b>
64-bit fully registered	9k
32-bit fully registered	7k
64-bit forward path registered	4k
32-bit forward path registered	3k
64-bit and 32-bit static bypass	0

———— **Note** —————

These gate count estimates do not include scan logic.



## 5 Signal descriptions

The AXI register slice uses standard AMBA AXI signals as described in the *AMBA AXI Protocol Specification*.

———— **Note** —————

In this section:

- The read channel and write channel signals are appended with:
  - the letter **M** for signals that connect to the component master interface
  - the letter **S** for signals that connect to the component slave interface.
- The upper value of some bus widths is provided as a name to indicate that the number of signal lines in the bus is derived from user-defined generics or parameters. These are described in the *PrimeCell Infrastructure AMBA 3 AHB Register Slice (BP130) Design Manual*.
- A number of user-defined signal lines are provided. These are named **xUSERM** or **xUSERS**, the letter **x** denotes the AXI channel and can be any of the following:
  - AW** Write address channel.
  - W** Write data channel.
  - B** Write response channel.
  - AR** Read address channel.
  - R** Read data channel.

The register slice signals are shown in:

- *Global AXI and scan signals*
- *Write channel signals* on page 10
- *Read channel signals* on page 11
- *Non-standard signals* on page 11.

### 5.1 Global AXI and scan signals

Figure 5 shows the register slice global AXI and scan signal connections.



**Figure 5 Global AXI and scan signal connections**

## 5.2 Write channel signals

Figure 6 shows the AXI write channel signal connections.

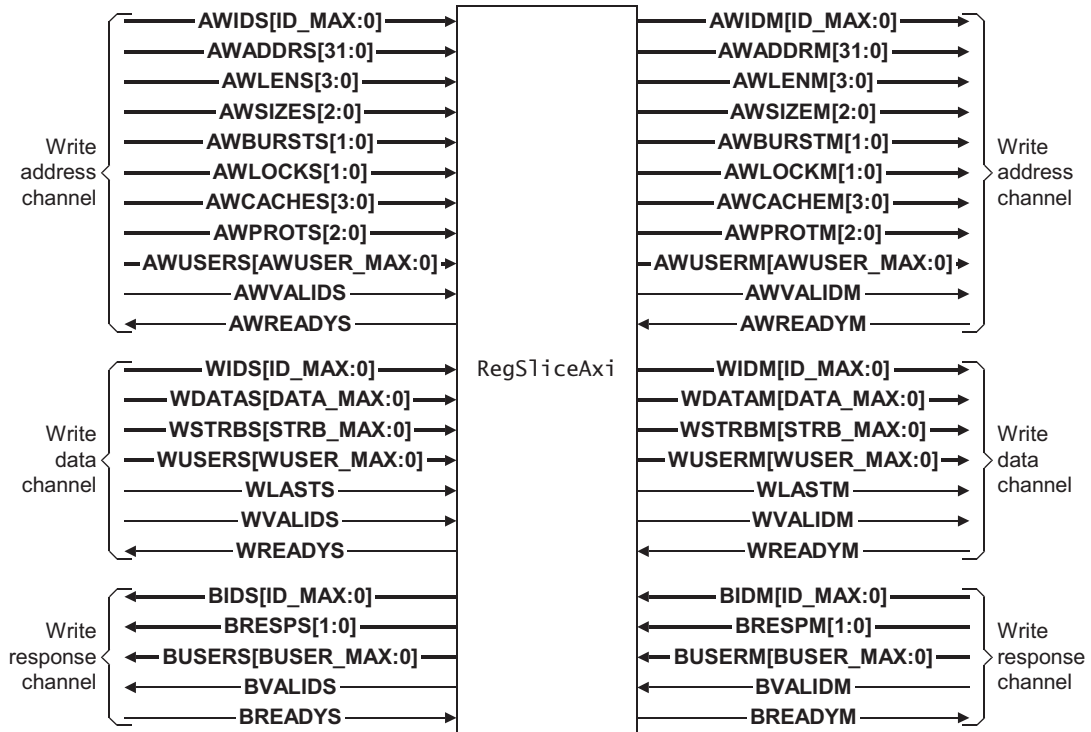


Figure 6 Write channel signal connections

### 5.3 Read channel signals

Figure 7 shows the AXI read channel signal connections.

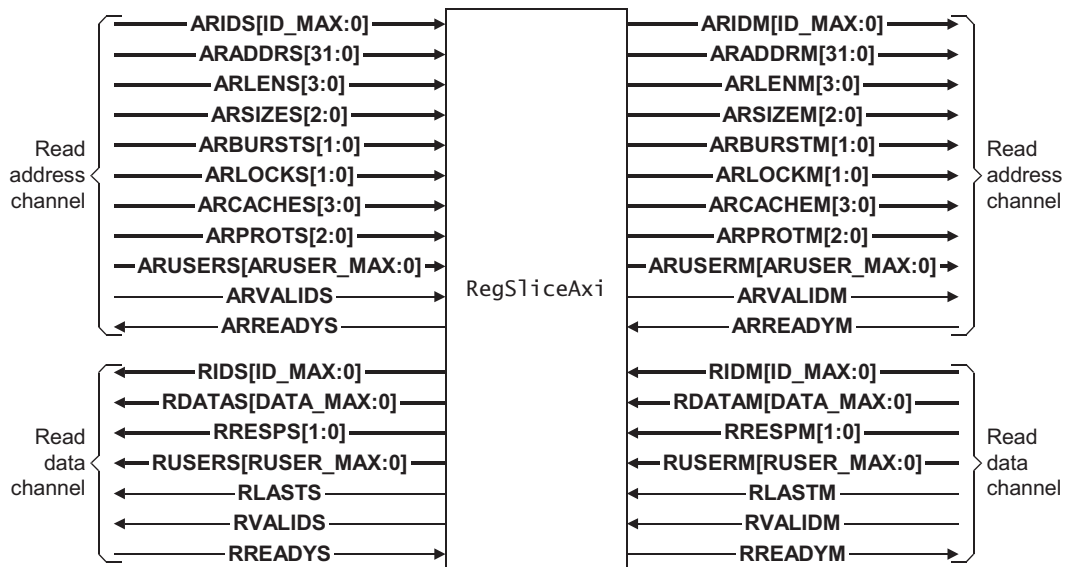


Figure 7 Read channel signal connections

### 5.4 Non-standard signals

Table 5 lists signals that are present on the register slice but are not described in the AXI specification.

Table 5 Non-standard signals

Name	Type	Source/ destination	Description
SCANENABLE	Input	Scan logic	Scan mode enable
SCANINACLK	Input	Scan logic	Scan chain input
SCANOUTACLK	Output	Scan logic	Scan chain output
AWUSERS	Input	AXI master	Additional sideband signals for the write address channel
WUSERS	Input	AXI master	Additional sideband signals for the write data channel
BUSERS	Output	AXI master	Additional sideband signals for the write response channel

**Table 5 Non-standard signals (continued)**

<b>Name</b>	<b>Type</b>	<b>Source/ destination</b>	<b>Description</b>
<b>ARUSERS</b>	Input	AXI master	Additional sideband signals for the read address channel
<b>RUSERS</b>	Output	AXI master	Additional sideband signals for the read data channel
<b>AWUSERM</b>	Output	AXI slave	Additional sideband signals for the write address channel
<b>WUSERM</b>	Output	AXI slave	Additional sideband signals for the write data channel
<b>BUSERM</b>	Input	AXI slave	Additional sideband signals for the write response channel
<b>ARUSERM</b>	Output	AXI slave	Additional sideband signals for the read address channel
<b>RUSERM</b>	Input	AXI slave	Additional sideband signals for the read data channel