ARM®

PrimeCell® Infrastructure AMBA™ 3 AXI Asynchronous Bridge (BP132) Revision: r0p1 **Technical Overview**

This technical overview describes the functionality of the AXI asynchronous bridge in the following sections:

1 Preliminary material

1.1 Release information

Table 1 lists the changes to this document.

Table 1 Change History

Date	Issue	Confidentiality	Change
07 October 2005	A	Non-Confidential	First release, for r0p0
26 January 2006	B	Non-Confidential	Second release, for r0p1

1.2 Proprietary notice

1.3 Confidentiality status

This document is Non-Confidential. This document can only be distributed in accordance with the terms set out in your license agreement.

1.4 Product status

The information in this document is final, that is for a developed product.

1.5 Web address

`http://www.arm.com`

2 About the AXI asynchronous bridge

The AXI asynchronous bridge, `AsyncAxi`, enables two AXI clock domains to communicate. Figure 1 shows `AsyncAxi` with data being transferred between two AXI clock domains.

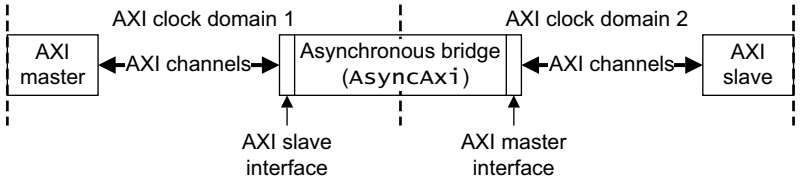

Figure 1 Asynchronous bridge block diagram

The bridge provides buffered synchronization of the AXI channels:

AW Write address channel.

W Write data channel.

B Write response channel.

AR Read address channel.

R Read data channel.

The HDL code is supplied as Verilog.

The major features of the bridge are:

- single independent AXI master and AXI slave interfaces
- all AXI channels are buffered independently
- configurable FIFO buffer depth for each AXI channel
- dynamic synchronous bypass mode.

The *PrimeCell Infrastructure AMBA 3 AXI Asynchronous Bridge (BP132) Design Manual* provides more information about these features.

3 Functional description

The following sections describe the bridge:

- *Operation*
- *Interface attributes* on page 5.

3.1 Operation

At the top level, the bridge comprises:

- five FIFOs, one for each AXI channel
- logic to manage transition to and from synchronous bypass mode.

There is no requirement for the bridge to examine any part of the data in an AXI channel, it can therefore be treated as unstructured and consider each channel as valid, ready, and payload data.

Figure 2 shows a block diagram of the major internal component blocks. The clock, reset, and scan pins are omitted for clarity.

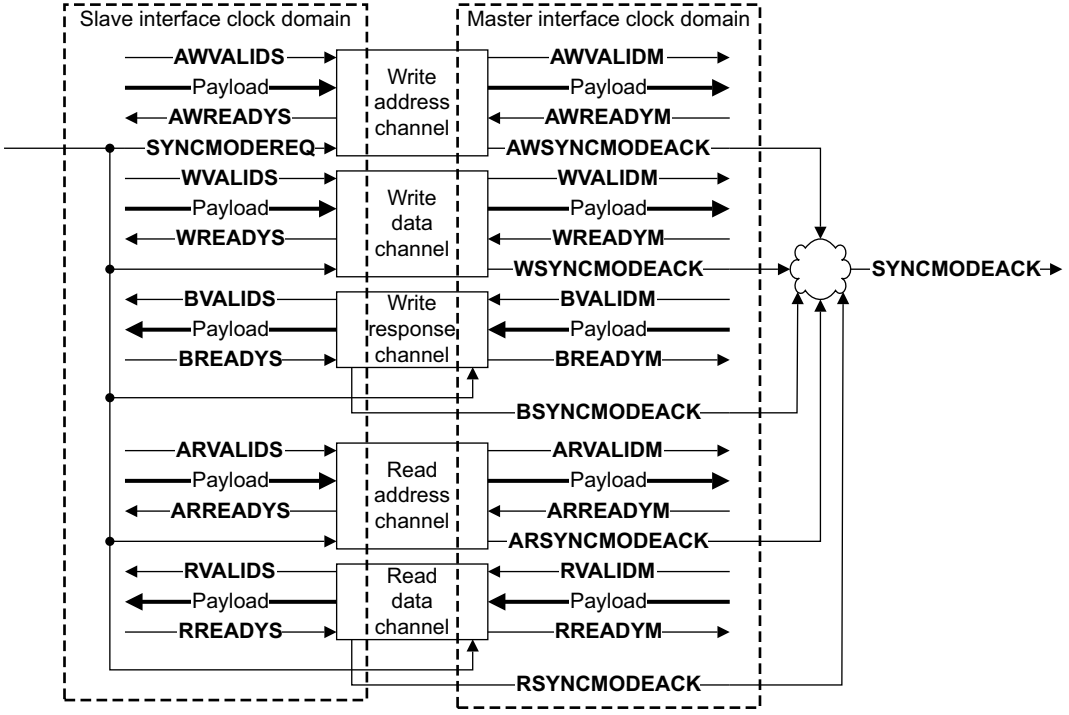

Figure 2 Asynchronous bridge components

Each channel FIFO is divided into two halves that correspond to the source of the clock for the components in them.

ACLKS Connects to the following:

- write address channel FIFO write half
- write data channel FIFO write half
- read address channel FIFO write half
- write response channel FIFO read half
- read data channel FIFO read half.

ACLKM Connects to the following:

- write address channel FIFO read half
- write data channel FIFO read half
- read address channel FIFO read half
- write response channel FIFO write half
- read data channel FIFO write half.

Two of the FIFOs operate in the opposite direction to the other three but all five behave in the same way with respect to their read and write halves.

The *PrimeCell Infrastructure AMBA 3 AXI Asynchronous Bridge (BP132) Design Manual* provides more information about the FIFOs.

3.2 Interface attributes

The following tables list the master and slave interface attributes for the bridge:

- Table 2
- Table 3 on page 6.

Table 2 Master interface attributes

Attribute	Description	Value
Combined issuing capability	The maximum number of active transactions that a master can generate	Master-dependent
Read ID capability	The maximum number of different **ARID** values that a master can generate for all active read transactions at any one time	Master-dependent
Read ID width	The number of bits in the **ARID** bus	Master-dependent
Read issuing capability	The maximum number of active read transactions that a master can generate	Master-dependent

Table 2 Master interface attributes (continued)

Attribute	Description	Value
Write ID capability	The maximum number of different **AWID** values that a master can generate for all active write transactions at any one time	Master-dependent
Write ID width	The number of bits in the **AWID** and **WID** buses	Master-dependent
Write issuing capability	The maximum number of active write transactions that a master can generate	Master-dependent

Table 3 Slave interface attributes

Attribute	Description	Value
Write acceptance capability	The maximum number of active write transactions that a slave can accept.	Slave-dependent
Read acceptance capability	The maximum number of active read transactions that a slave can accept.	Slave-dependent
Combined acceptance capability	The maximum number of active transactions that a slave can accept. You must specify this if read and write address storage is combined.	Slave-dependent
Write interleave depth	The number of active write transactions for which the slave can receive data. This is counted from the earliest transaction.	Slave-dependent
Read data reorder depth	The number of active read transactions for which a slave can transmit data. This is counted from the earliest transaction.	Slave-dependent

Note

The master-dependent and slave-dependent values in the Value column of Table 2 on page 5, and Table 3 indicate that the bridge adopts the attribute value of the master or slave that the interface is connected to.

4 Physical data

This section describes:

- *AC characteristics*
- *Gate count*.

4.1 AC characteristics

The asynchronous bridge adheres to the following timing guidelines. The figures relate to the percentage of clock cycle permitted for each function:

- AXI inputs must be valid for 40% prior to the rising edge of the clock.
- AXI outputs shall be valid by 20% after the rising edge of the clock.
- Combinatorial paths occupy no more than 9% of the clock cycle. There are no combinatorial through paths in the bridge except when it is in synchronous bypass mode. The multiplexing and demultiplexing of the signals from one side of the bridge to the other in synchronous bypass mode is synthesized as a combinatorial path.

Performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process, at a target speed of 200MHz, confirms the timing characteristics.

4.2 Gate count

The total gate-count with the default configuration that Table 4 shows, and scan chain insertion performed, is approximately 12600 NAND2X1-equivalent gates with the library that *AC characteristics* describes. Higher buffer depths in any of the AXI channels increase the gate count, and lower buffer depths decrease the gate count.

Table 4 Default FIFO buffer depths

AXI channel	Default	Legal range
Write address	2	1-8
Write data	4	1-8
Write response	2	1-8
Read address	2	1-8
Read data	4	1-8

5 Signal descriptions

Table 5 lists the non-standard AXI and scan signals.

Table 5 Non-standard AXI and scan signals

Name	Type	Description
ACLKM	Input	Master interface clock
ACLKS	Input	Slave interface clock
ARESETMn	Input	Master interface reset
ARESETSn	Input	Slave interface reset
AWUSERM	Output	Additional master interface signals for the write address channel
AWUSERS	Input	Additional slave interface signals for the write address channel
WUSERM	Output	Additional master interface signals for the write data channel
WUSERS	Input	Additional slave interface signals for the write data channel
BUSERM	Input	Additional master interface signals for the write response channel
BUSERS	Output	Additional slave interface signals for the write response channel
ARUSERM	Output	Additional master interface signals for the read address channel
ARUSERS	Input	Additional slave interface signals for the read address channel
RUSERM	Input	Additional master interface signals for the read data channel
RUSERS	Output	Additional slave interface signals for the read data channel
SYNCMODEACK	Output	Synchronous bypass mode acknowledge
SYNCMODEREQ	Input	Synchronous bypass mode request
SCANENABLE	Input	Scan logic common scan mode enable
SCANINACLKM	Input	Scan logic master interface clock domain scan chain input
SCANINACLKS	Input	Scan logic slave interface clock domain scan chain input
SCANOUTACLKM	Output	Scan logic master interface clock domain scan chain output
SCANOUTACLKS	Output	Scan logic slave interface clock domain scan chain output

Figure 3 on page 10 shows the AXI asynchronous bridge signal connections.

Note

In Figure 3 on page 10:

- The read channel, write channel, and low-power interface signals are standard AMBA AXI signals that the *AMBA AXI Protocol Specification* describes. The signal names are appended with:
  - the letter **M** for signals that connect to the component master interface
  - the letter **S** for signals that connect to the component slave interface.
- The scan signals are not shown.

The bridge has no low-power interface signals because it has no low power mode and does not initiate AXI transactions.

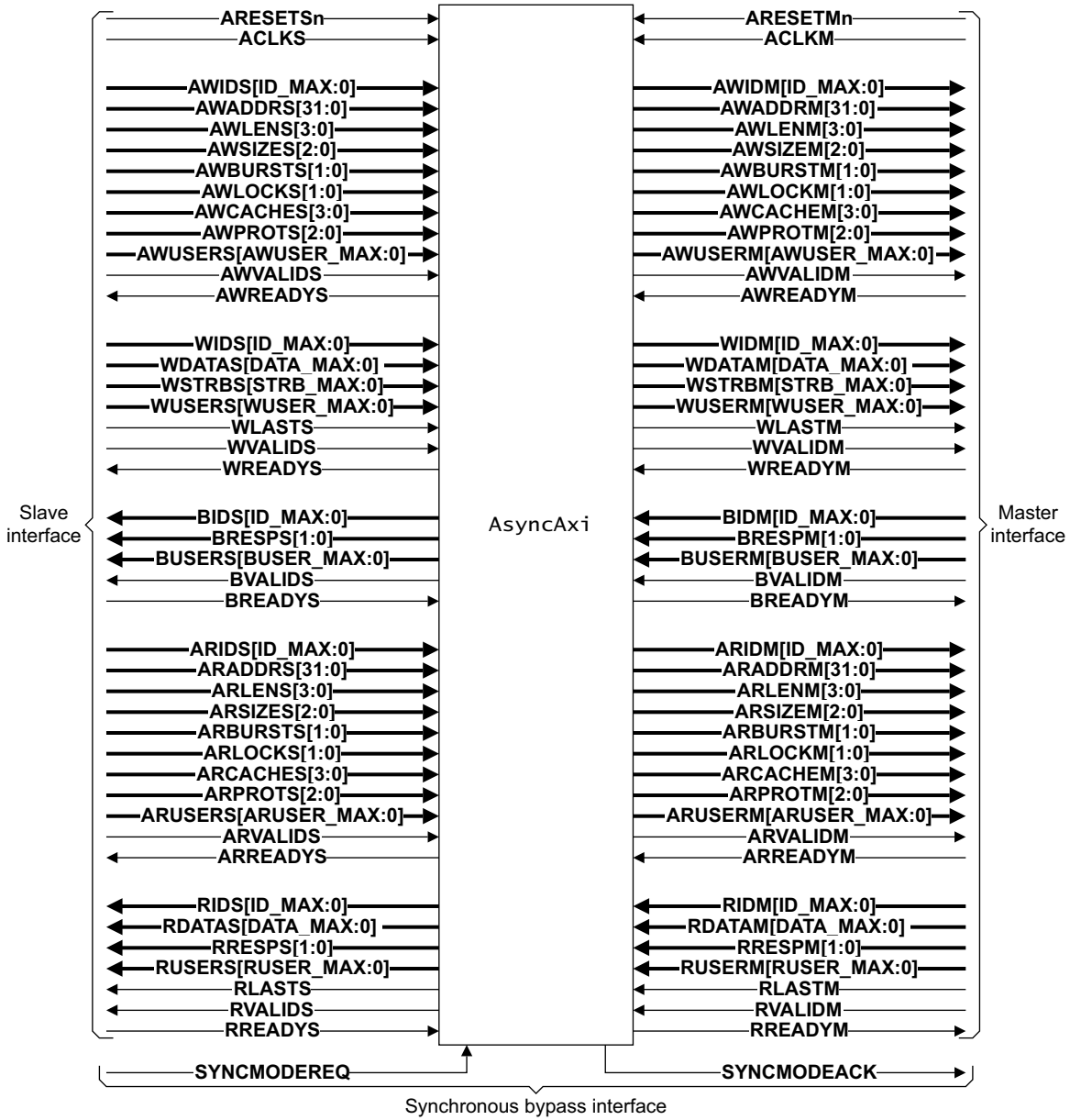

Figure 3 Asynchronous bridge signal connections

