Logic Expansion Card
(KPI-0045A)
User Guide
Logic Expansion Card
User Guide

Change log

<table>
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<tr>
<th>Date</th>
<th>Issue</th>
<th>Change</th>
</tr>
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<tr>
<td>July 1998</td>
<td>A</td>
<td>First release</td>
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Preface
Logic Expansion Card

About this document

This document describes the Logic Expansion Card (KPI-0045A) which is used with the ARM Development Board to allow you to prototype peripherals around an ARM core.

Intended audience

This document has been written for experienced engineers who have knowledge of the bus architecture (AMBA), coprocessor interfaces, and the ARM core they are working with.

How to use this document

This document is split into the following four sections:

- Chapter 1 Overview. This gives a brief description of the Logic Expansion Card, its main features and how to connect it to the ARM Development Board.
- Chapter 2 Hardware Description. This gives a description of the main areas of the Logic Expansion Card.
• Chapter 3 Configuring the Logic Expansion Card. This gives details of the jumpers and links on the Logic Expansion Card that you have to set.

• Appendix A Schematics. This comprises the circuit diagram, layout diagram, and connector diagrams of the Logic Expansion Card.

Typographical conventions

The following typographical conventions are used in this document:

**bold** highlights signal names within text

*italic* highlights important notes, ARM-specific terminology, cross references, and references to other publications

Abbreviations

The following abbreviations are used in this document:

**AMBA** Advanced Microcontroller Bus Architecture. This specification defines an on-chip communications standard for designing high performance 32-bit and 16-bit embedded microcontrollers.

**FPGA** Field Programmable Gate Array. This is a type of programmable logic device.

**PLD** Programmable Logic Device.

**PLL** A Phase Locked Loop. This usually comprises:

• a voltage controlled oscillator
• a programmable divider
• a phase comparator
• an integrator.

These components allow a programmable clock to be generated. This clock is locked and stabilized by a reference clock input.

**VHDL** This is a Hardware Description Language suitable for the simulation and synthesis of logic circuits.

**Test chip** A test chip is an implementation of the ARM core without peripherals, manufactured primarily to validate the porting of the ARM core to a new process. For further details on test chip documentation refer to Related publications.

**ICE** An In-Circuit Emulator.
EmbeddedICE  This is a debugging system used to provide many functions of an ICE, consisting of:

- an on-chip macrocell
- an interface unit
- software.

Related publications

The following ARM documents may be useful:

- The ARM Target Development System User Guide (ARM DUI 0061)
- The AMBA Specification (ARM IHI 0001)

In addition, you may find it useful to refer to the ARM Datasheet, ARM Test Chip Appendix, and header card documents appropriate to the processor you are using. For details on which documents are available please contact ARM Limited, or refer to ARM’s website at http:\www.arm.com.

Feedback on this document

If you have any comments or suggestions about this document, please contact your supplier giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- a concise explanation of your comments.
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Chapter 1
Overview

1.1 Introduction

The ARM Development Board helps you to develop ASICs based on embedded ARM processors, and provides a convenient means of evaluating ARM’s family of RISC processors.

The Logic Expansion Card is a useful addition to the ARM Development Board. It provides a large amount of programmable, uncommitted logic in the form of two large FPGAs. This allows you to evaluate the proposed logic of an ASIC’s design.

You can synthesize either AMBA or coprocessor-based peripherals into these FPGAs, allowing you to develop and test device drivers for the peripherals in an ASIC early in your design cycle.

The hardware and software described in this document can be used with any ARM test chip that can be fitted to the ARM Development Board.
1.2 System requirements

To use the Logic Expansion Card you will need the following:

- ARM Development Board (HBI-0011B).
- An ARM Processor Header Card. At the time of printing the Logic Expansion Card supports the following Processor Header Cards:
  - ARM710T header card (HHI-0033)
  - ARM720T header card (HHI-0031)
  - ARM740T header card (HHI-0038)
  - ARM9TDMI header card (HHI-0016)
  - ARM940T header card (HHI-0032)
  - ARM9TDMI header card (HHI-0045)
If you have a Processor Header Card not listed above, please contact ARM Limited to check compatibility.

- ARM Debugger, such as:
  - Mulit-ICE (recommended)
  - EmbeddedICE
  - Angel

- A synthesis tool, such as Exemplar.

- Xilinx tools (M1.4 or greater) are required to place and route the design.

1.3 Features of the Logic Expansion Card

The main features of the Logic Expansion Card are:

- Two FPGAs. These allow peripherals that are based on AMBA or coprocessor interfaces to be synthesized into uncommitted logic.

- A programmable PLL. This generates the fast processor clock, $FCLK$, and is programmed via jumpers on the Logic Expansion Card.

- A 50ohm mini-coax connector. This allows you to input an external clock signal.

- A general purpose input/output connector. This is an expansion connector which allows you to expand the board, or debug using non-ARM tools.

- The ability to separate core and pad power supplies. This allows you to measure the power requirements of just the ARM processor core.
1.4 Connecting the Logic Expansion Card

The Logic Expansion Card is fitted between the ARM Development Board and the Processor Header Card (see Figure 1-1 Connecting the Logic Expansion Card). This allows the signals between the ARM Development Board and the Processor Header Card to be intercepted if necessary.

When fitted, the Logic Expansion Card protrudes over the edge of the ARM Development Board and Processor Header Card, so that you can access the jumpers without having to remove the header card.

![Figure 1-1 Connecting the Logic Expansion Card](image-url)
1.5 Using the Logic Expansion Card

The floppy disc supplied with the Logic Expansion Card contains guidance and an example designed to help you use the Logic Expansion Card. The file Readme.pdf on the disc contains:

- an example of a simple memory-mapped peripheral for the Logic Expansion Card
- a procedure on how to use the example
- guidelines on how to implement your own design
- a list of associated files contained on the disc.

Readme.pdf can be viewed using Adobe Acrobat Reader version 3.0—you can download a copy of this free of charge from the Documentation area on ARM’s website (http:\\www.arm.com)
Chapter 2
Hardware Description

This chapter describes the following areas of the Logic Expansion Card:
• Header Card connectors (page 2-2)
• Power supply (page 2-2)
• Clock generation (page 2-3)
• FPGA configuration (page 2-4)
• General purpose input/output connection (expansion connector) (page 2-6)
• Status LEDs (page 2-7).

The circuit diagram, layout diagram and connector diagrams are detailed in Appendix A.
2.1 Header card connectors

The Logic Expansion Card has five 60-way header card connectors (PL1–PL5).

- Four of the connectors (PL1–PL4) connect to both the ARM Development Board and the Processor Header Card, and the majority of the connections carry signals from the development board straight through to the header card, with a connection to one, or both of the FPGAs. These connectors also carry additional signals from the Logic Expansion Card to the Processor Header Card. These additional signals are:
  - coprocessor signals
  - instruction buses
  - miscellaneous signals.

- The fifth connector (PL5) connects to the Processor Header Card only, and carries coprocessor signals that are required by certain ARM devices (for example, ARM940T has additional coprocessor signals that are not available on the other connectors (PL1–PL4)).

2.2 Power supply

The Logic Expansion Card takes its power from the 3.3V supply on the ARM Development Board. All the supplies are decoupled, and low ESR capacitors are used throughout.

The ARM Development Board provides protection from 5V signals, which means the Logic Expansion Card supports ARM processors operating over the range 2.7V–5V. The Logic Expansion Card allows you to measure the core power consumption as the power supply (Vdd) is split into:

- Core power supply (Vddm)
- Pad power supply (Vdd).

If you want to vary the power supply to the core in order to make current measurements, you must remove the link JP1 and connect an external power supply. Alternatively, you can replace JP1 with a low value resistor (for example a 1ohm resistor) and measure the voltage across it.
2.3 Clock generation

The Logic Expansion Card uses two clocks:
- BCLK
- FCLK.

2.3.1 BCLK

BCLK is the AMBA bus clock, and is generated on the ARM Development Board. This clock can be set to one of the following frequencies:
- 4MHz
- 8MHz
- 16MHz
- 20MHz.

For details on how to set the frequency of BCLK refer to the *ARM Target Development System User Guide* (ARM DUI 0061).

2.3.2 FCLK

FCLK is used to clock the two FPGAs on the Logic Expansion Card. You have the option of using three different sources for FCLK:
- Generated on the Processor Header Card
- Input from an external source
- Generated on the Logic Expansion Card.

For details on how to select which source to use refer to *Table 3-2 Selecting and setting FCLK* on page 3-4.

**FCLK—generated on the Processor Header Card**

If you are using FCLK generated on the Processor Header Card refer to the User Guide supplied with that card for details on the frequencies available, and how to set them.

**FCLK—input from an external source**

If you are using an external FCLK, you need to connect it to the 50ohm mini-coax connector SK5.
Hardware Description

**FCLK—generated on the Logic Expansion Card**

A PLL (AV9155-02 or W48C55-62) is provided on the Logic Expansion Card which generates a local FCLK. This clock is used to drive the two FPGAs, and can be used to drive FCLK on the Processor Header Card.

The reference clock to the on-board PLL is supplied by a crystal which has a frequency of 14.318MHz.

The on-board PLL has three programmable inputs, and can output one of 12 preset frequencies in the range 4–100MHz.

In addition to these 12 preset frequencies you can set the output of the PLL to be the same value as the AMBA bus clock generated by the ARM Development Board. See 2.3.1 BCLK on page 2-3. If you set FCLK to equal BCLK then any changes to the BCLK value will result in a change to the FCLK value.

For details on the frequencies available and how to set them refer to Table 3-2 Selecting and setting FCLK on page 3-4.

### 2.4 FPGA configuration

The Logic Expansion Card has two FPGAs:

- U9, for connection to the AMBA bus
- U10, for connection to the coprocessor interface.

Both of these are 240-pin PQFP XILINX (3.3V) FPGAs (XC4062XL), which provides enough input/output pins and resources to enable you to prototype most peripherals. A 72-bit bus is provided as a communication channel between the two FPGAs, and you can use this bus to drive the eight general-purpose LEDs. (See 2.6 Status LEDs on page 2-7.)

You can load the content of the FPGAs from either:

- separate serial PROMs
- via an XChecker cable.

Full details are given in the following sections, 2.4.1 and 2.4.2 and Figure 2-1 shows the position of the PROMs, connectors and link positions associated with configuring the FPGAs.
2.4.1 Loading from PROM

To enable you to load the content of the FPGAs from PROM, the Logic Expansion Card has two pairs of PROM sockets—one pair for the AMBA FPGA (U1 and U3) and one for the coprocessor interface FPGA (U5 and U6). Each pair is serially connected, which allows them to be cascaded.

Each pair may comprise:
- a single 1MB PROM (XC1701L)
- a single 1MB PROM (XC1701L), cascaded with a single 512KB PROM (XC17512L)
- two 1MB PROMs (XC1701L) cascaded together.

To set the Logic Expansion Card to load the AMBA FPGA from PROM you must fit jumper J4. To set the Logic Expansion Card to load the coprocessor interface FPGA from PROM you must fit jumper J6.
2.4.2 Loading via an XChecker cable

To enable you to load the content of the FPGAs via an XChecker cable the Logic Expansion Card has two 9-pin connectors—one for the AMBA FPGA (J1) and one for the coprocessor interface FPGA (J2).

To allow the bit files to be downloaded to the PROMs you have to run the Xilinx Hardware Debugger portion of the Xilinx M1 software.

Caution

Before using the XChecker cable you must remove the appropriate PROMs (either U1 and U3, or U5 and U6).

You must use the 3V adaptor board supplied with the XChecker cable to provide 5V to the XChecker cable.

To set the Logic Expansion Card to load the AMBA FPGA via an XChecker cable you must remove jumper J4. To set the Logic Expansion Card to load the coprocessor interface FPGA via an XChecker cable you must remove jumper J6.

2.5 Expansion connector

The Logic Expansion Card has a 96-pin expansion connector (J3). This connector provides access to the signal bus which is shared by both the AMBA FPGA and the coprocessor interface FPGA.

The internal signals in the FPGA can be routed directly to the expansion connector allowing you to:
• monitor the signals (logic analyzer probes can easily be attached)
• use it as a platform to prototype small peripherals
• develop expansion boards.

The signals are divided into the following three buses:
• 32-bit address bus FA[31:0]
• 32-bit data bus FD[31:0]
• 8-bit control bus FC[7:0]

The expansion connector also supplies +3.3V power and ground. For details of the pinout refer to Table A-1 Expansion connector — Pinout on page A-13.
2.6 Status LEDs

The Logic Expansion Card has ten surface mount status LEDs (D1–D10):

- D1–D8. These yellow LEDs, when enabled, indicate the status of the FPGAs. You can configure these yellow LEDs (via the link LK3) to be:
  - disabled—link fitted between A and C
  - permanently enabled—link fitted between B and C
  - enabled, where they are buffered under AMBA FPGA control (nLEDEN on pin 233 of the AMBA FPGA)—link removed

- D9–D10. These green LEDs indicate if the FPGAs have loaded their configuration data correctly (D9 for the AMBA FPGA and D10 for the coprocessor interface FPGA).

The LEDs are buffered by U8 and light with a logic 0 on the control bus FC[7:0].

2.7 BERROR

If the processor fitted in the Processor Header Card attempts to access a memory map address above 256MB, the ARM Development Board generates a BERROR signal which is passed back to the header card causing the processor to perform a data abort.

If you require access to memory map addresses above 256MB you must develop logic for the AMBA FPGA. This logic must allow BERROR to be intercepted and generate a ERROROUT signal only if the higher address value is exceeded. ERROROUT received by the header card will cause the processor to perform a data abort. To enable the interception of BERROR you must remove the link J10.

2.8 BLAST

The ARM Development Board generates a BLAST signal to indicate a non-sequential cycle. If the header card receives a combination of BLAST and BERROR signals it causes a retract bus operation.

The Logic Expansion Card allows you to configure the card such that BLAST is intercepted by the AMBA FPGA. To enable the interception of BLAST you must remove the link J11.

--- Note ---

It is recommended that you fit the J11, and disable the interception of BLAST.
Chapter 3
Configuring the Logic Expansion Card

The Logic Expansion Card is configurable via:
• a wire fitted link (JP1)
• eleven jumpers (J1, J2, J4–J12)
• two sets of links (LK1 and LK2)
• one surface mount link (LK3).

Section 3.1 shows the location of the jumpers and links, section 3.2 gives a brief description for each jumper and link, and section 3.3 gives details of how to select and set FCLK using LK1 and LK2.
3.1 Locating jumpers and links

Figure 3-1 Location of jumpers and links
## 3.2 Summary of jumper and link settings

<table>
<thead>
<tr>
<th>Jumper/link</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J5</td>
<td>Not used. *</td>
</tr>
<tr>
<td>J6</td>
<td>If fitted the coprocessor interface FPGA is loaded from PROM. If removed the coprocessor interface FPGA is loaded via an XChecker cable.</td>
</tr>
<tr>
<td>J7</td>
<td>Not used. *</td>
</tr>
<tr>
<td>J8</td>
<td>Not used. *</td>
</tr>
<tr>
<td>J9</td>
<td>Not used. *</td>
</tr>
<tr>
<td>J10</td>
<td>If fitted, the AMBA FPGA does not implement the interception of BERROR. If removed, the AMBA FPGA intercepts BERROR from the ARM Development Board. (For details refer to 2.7 BERROR on page 2-7)</td>
</tr>
<tr>
<td>J11</td>
<td>If fitted, the AMBA FPGA does not implement the interception of BLAST. If removed, the AMBA FPGA intercepts BLAST from the ARM Development Board. (For details refer to 2.8 BLAST on page 2-7)</td>
</tr>
<tr>
<td>J12</td>
<td>Not used. *</td>
</tr>
<tr>
<td>LK1 and LK2</td>
<td>Used to select the source and frequency of FCLK. For details refer to Table 3-2 Selecting and setting FCLK on page 3-4</td>
</tr>
<tr>
<td>LK3</td>
<td>Used to control the output buffer used to drive the eight status LEDs (D1—D8). If fitted between A and C, the LEDs are disabled. If fitted between B and C, the LEDs are enabled. If removed, the LEDs are buffered under FGPA control (nLEDEN on pin 233 of the AMBA FPGA). This is the factory default.</td>
</tr>
</tbody>
</table>

* The jumpers J5, J7–J9, and J12 may be used to provide access to the spare FGPA inputs/outputs. You may use these as extra monitoring points, or allow the FPGA to read them to provide configuration options.
## 3.3 Selecting and setting FCLK

### Table 3-2 Selecting and setting FCLK

<table>
<thead>
<tr>
<th>Source</th>
<th>FCLK Source (MHz)</th>
<th>FREQ LK0</th>
<th>FREQ LK1</th>
<th>FREQ LK2</th>
<th>Do not fit</th>
<th>MCLK</th>
<th>CLK</th>
<th>2XCLK</th>
<th>EXTCLK</th>
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<td>OUT</td>
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<td>OUT</td>
<td>OUT</td>
<td>OUT</td>
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<td>External</td>
<td>-</td>
<td>OUT/IN</td>
<td>OUT/IN</td>
<td>OUT/IN</td>
<td>-</td>
<td>OUT</td>
<td>OUT</td>
<td>OUT</td>
<td>IN</td>
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<tr>
<td>ARM Development Board = BCLK</td>
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<td>OUT/IN</td>
<td>OUT/IN</td>
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</tbody>
</table>
Appendix A
Schematics

This Chapter contains the following illustrations and tables:

• Figure A-1 Component layout on page A-2.
• Figure A-2 Top level schematic on page A-3.
• Figure A-3 AMBA FPGA — Schematic on page A-4.
• Figure A-4 AMBA FPGA — Pin layout on page A-5.
• Figure A-5 Coprocessor interface FPGA — Schematic on page A-6.
• Figure A-6 Coprocessor interface FPGA — Pin layout on page A-7.
• Figure A-7 Clock generation — Schematic on page A-8.
• Figure A-8 Status LEDs — Schematic on page A-9.
• Figure A-9 Lower header connectors — Schematic on page A-10.
• Figure A-10 Upper header connectors — Schematic on page A-11.
• Figure A-11 Expansion connector — Pin location on page A-12.
• Figure A-12 Expansion connector — Pinout schematic on page A-12.
• Table A-1 Expansion connector — Pinout on page A-13.
A.1 Component layout

Figure A-1 Component layout
A.2 Top level schematic

Figure A-2 Top level schematic

Note: Insert link only when FPGAs are not programmed or design does not use BERROR.
A.3 Amba FPGA schematic and pin layout

Figure A-3 AMBA FPGA — Schematic
Figure A-4 AMBA FPGA — Pin layout
A.4  Coprocessor interface FPGA schematic and pin layout

Figure A-5 Coprocessor interface FPGA — Schematic
Figure A.6 Coprocessor interface FPGA – Pin layout
A.5 Clock generation schematic

Figure A-7 Clock generation — Schematic
A.6 Status LEDs schematic

Figure A-8 Status LEDs — Schematic
A.7 Header connectors schematics

Figure A-9 Lower header connectors — Schematic
Figure A-10: Upper header connectors — Schematic
A.8 Expansion connector pin location, schematic and pinout

Figure A-11 Expansion connector — Pin location

Figure A-12 Expansion connector — Pinout schematic
### Table A-1 Expansion connector — Pinout

<table>
<thead>
<tr>
<th>Row A</th>
<th>Row B</th>
<th>Row C</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD0</td>
<td>FC0</td>
<td>FA31</td>
</tr>
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<td>FC1</td>
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<tr>
<td>FD2</td>
<td>FC2</td>
<td>FA29</td>
</tr>
<tr>
<td>FD3</td>
<td>FC3</td>
<td>FA28</td>
</tr>
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