ARM® LogicTile Express 13MG

V2F-2XV6

Technical Reference Manual

ARM®

ARM DUI 0556G (ID052914)

ARM LogicTile Express 13MG
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
21 September 2010	A	Non-Confidential	First release
28 March 2011	B	Non-Confidential	Second Release
22 June 2012	C	Non-Confidential	Third Release
12 October 2012	D	Non-Confidential	Fourth Release
31 March 2013	E	Non-Confidential	Fifth Release
29 October 2013	F	Non-Confidential	Sixth Release
28 May 2014	G	Non-Confidential	Seventh Release

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

CE

The system should be powered down when not in use.

The LogicTile Express 13MG generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the card.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note

It is recommended that wherever possible shielded interface cables be used.

Contents
ARM LogicTile Express 13MG Technical Reference Manual

Preface

This is the *Technical Reference Manual* (TRM) for the *LogicTile Express 13MG*. It contains the following sections:

About this book

This book is for the LogicTile Express 13MG, V2F-2XV6, daughterboard.

Intended audience

This book is written for experienced hardware and software engineers who are developing ARM-based products using the daughterboard as part of a Versatile™ Express development platform.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the daughterboard.

Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the LogicTile Express 13MG daughterboard.

Appendix A *Signal Descriptions*

Read this for a description of the signals present at the external interface connectors of the daughterboard.

Appendix B *Specifications*

Read this for the electrical specifications of the daughterboard.

Appendix C *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM® Glossary*, http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Typographical conventions

Conventions that this book can use are described in:

- *Typographical*
- *Timing diagrams* on page viii
- *Signals* on page viii.

Typographical

The typographical conventions are:

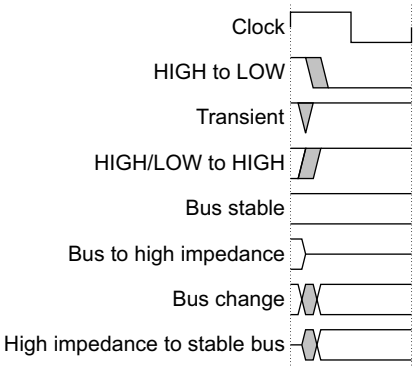
italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace italic`	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
< and >	Enclose replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

- See *ARM Information Center*, http://infocenter.arm.com/help/index.jsp for access to ARM documentation.
- See *ARM Technical Support Knowledge Articles*, http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html for additional technical support.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- Application note AN233 *LogicTile Express 13MG example design for a CoreTile Express A9x4*
- *ARM® Motherboard Express µATX Technical Reference Manual* (ARM DUI 0447)
- *ARM® Versatile™ Express Configuration Technical Reference Manual* (ARM DDI 0496)
- *ARM® Programmer Module (V2M-CP1)* (ARM DDI 0495)
- *ARM® CoreTile Express A5x2 Technical Reference Manual* (ARM DUI 0541)
- *ARM ® CoreTile Express A15x2 Technical Reference Manual* (ARM DUI 0604)
- *ARM® CoreTile Express A9x4 Technical Reference Manual* (ARM DUI 0448)
- *ARM® LogicTile Express 3MG Technical Reference Manual* (ARM DUI 0449)
- *ARM® Versatile™ Express Boot Monitor Reference Manual* (ARM DUI 0465).

Other publications

This section lists relevant documents published by third parties:

- See the JEDEC Solid State Technology Association web site, www.jedec.org for information on *Small Outline Dual In-line Memory Modules* (SO-DIMM).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- the title
- the number, ARM DUI 0556G
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Chapter 1
Introduction

This chapter provides an introduction to the LogicTile Express 13MG daughterboard. It contains the following sections:

1.1 Precautions

This section contains advice about how to prevent damage to your daughterboard.

1.1.1 Ensuring safety

The daughterboard is powered from 12V DC through a 6 pin PCIe connector, U51. 5VDC and a *Variable IO* (VIO) voltage is supplied to the board through header connector HDRYL, J2, on the lower side of the board.

Warning

Do not use the daughterboard near equipment that is sensitive to electromagnetic emissions, for example medical equipment.

1.1.2 Preventing damage

The daughterboard is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure which leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

Caution

To avoid damage to the board, observe the following precautions.

- You must connect the PCIe power cable to the daughterboard before power-up to prevent damage.
- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Ensure that the voltage on the pins of the FPGA and interface circuitry on the daughterboard is at the correct level. Some of the daughterboard FPGA signals are connected directly to the Versatile Express µATX Motherboard.
- You must not configure FPGA pins connected to an external signal source as outputs.
- Do not use the board near a transmitter of electromagnetic emissions.

1.2 About the LogicTile Express 13MG daughterboard

The daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA®) that use the *Advanced eXtensible Interface* (AXI™) or custom logic for use with ARM processors.

Note

The daughterboard is designed only to be used with a Versatile Express µATX Motherboard.

The daughterboard contains the following devices:

- Two Xilinx Virtex-6 FPGAs, XC6VLX760, and XC6VLX550T:
  - Speed grade -1.
- Two Flash memories for FPGA images, one for each FPGA.
- Two Daughterboard Configuration Controllers to configure the FPGAs, one for each FPGA.
- 16MB of on-board 32-bit ZBT RAM, two independent banks of 8MB each.
- Up to 4GB of external DDR2 64-bit memory using *Small Outline Dual In-line Memory Module* (SO-DIMM).
- HDRXL header on the bottom side of the board with two *High-Speed Buses* (HSB), one Master, one Slave, that connect to the other daughterboard site.
- HDRYL header on the bottom side of the board with five buses to the motherboard.
- HDRXU and HDRYU headers on the top side of the board for expansion.
- *Serial Advanced Technology Attachment* (SATA) Host (H) and Device (D) connectors.
- JTAG and Trace debug interfaces.
- Eight general-purpose *Dual In-line Package* (DIP) switches.
- 22 status and user LEDs:
  - Eight green user LEDs connected to each Daughterboard Configuration Controller.
  - One green user LED connected to each FPGA.
  - One green status LED for each FPGA indicating *FPGA configured*.
  - One red status LED for each FPGA indicating *FPGA over temperature*.

Figure 1-1 on page 1-4 and Figure 1-2 on page 1-5 show the physical layout of the daughterboard.

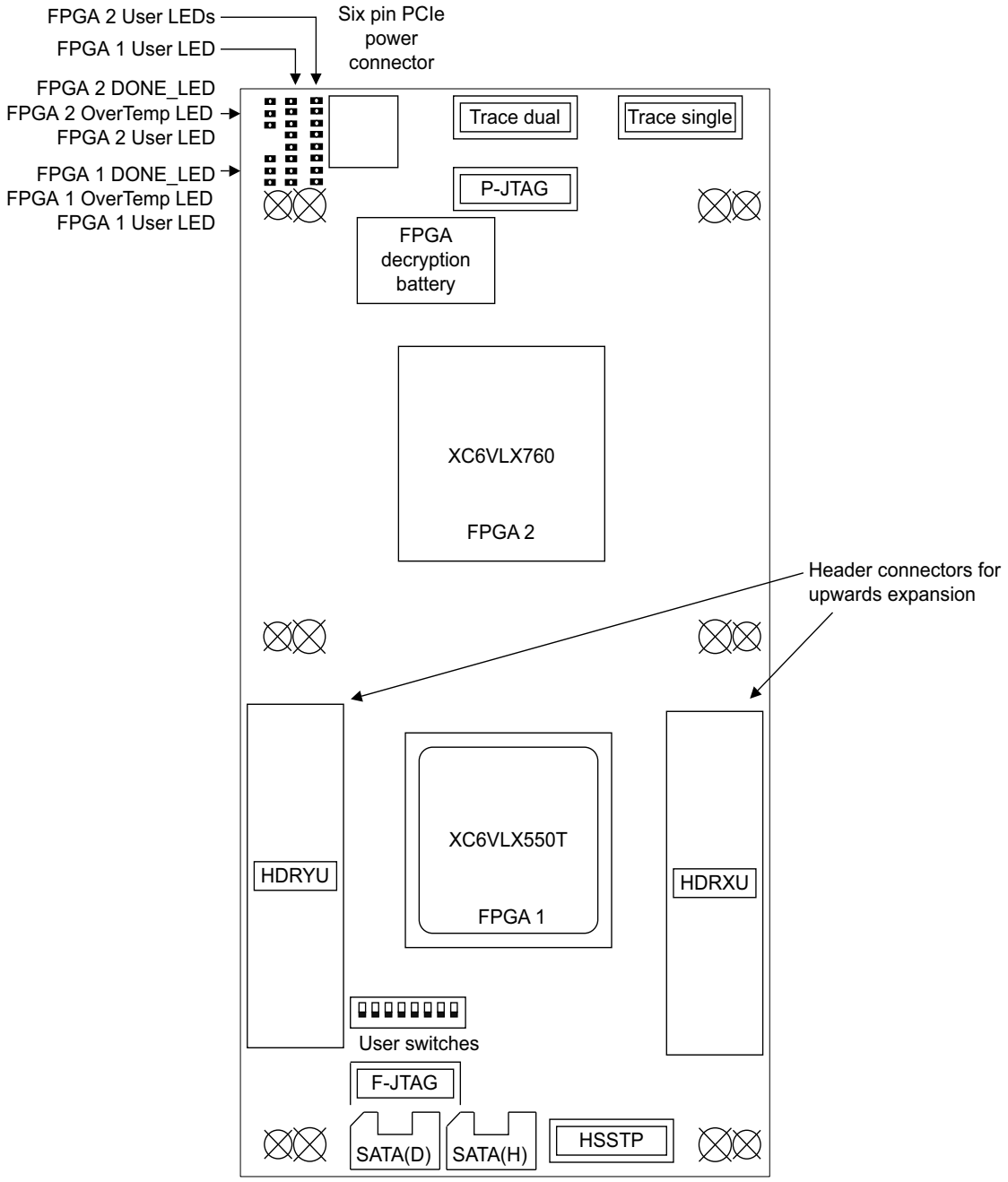


Figure 1-1 Daughterboard layout, top

Note

When the daughterboard is fitted to the motherboard, the top side of the board faces away from the motherboard.

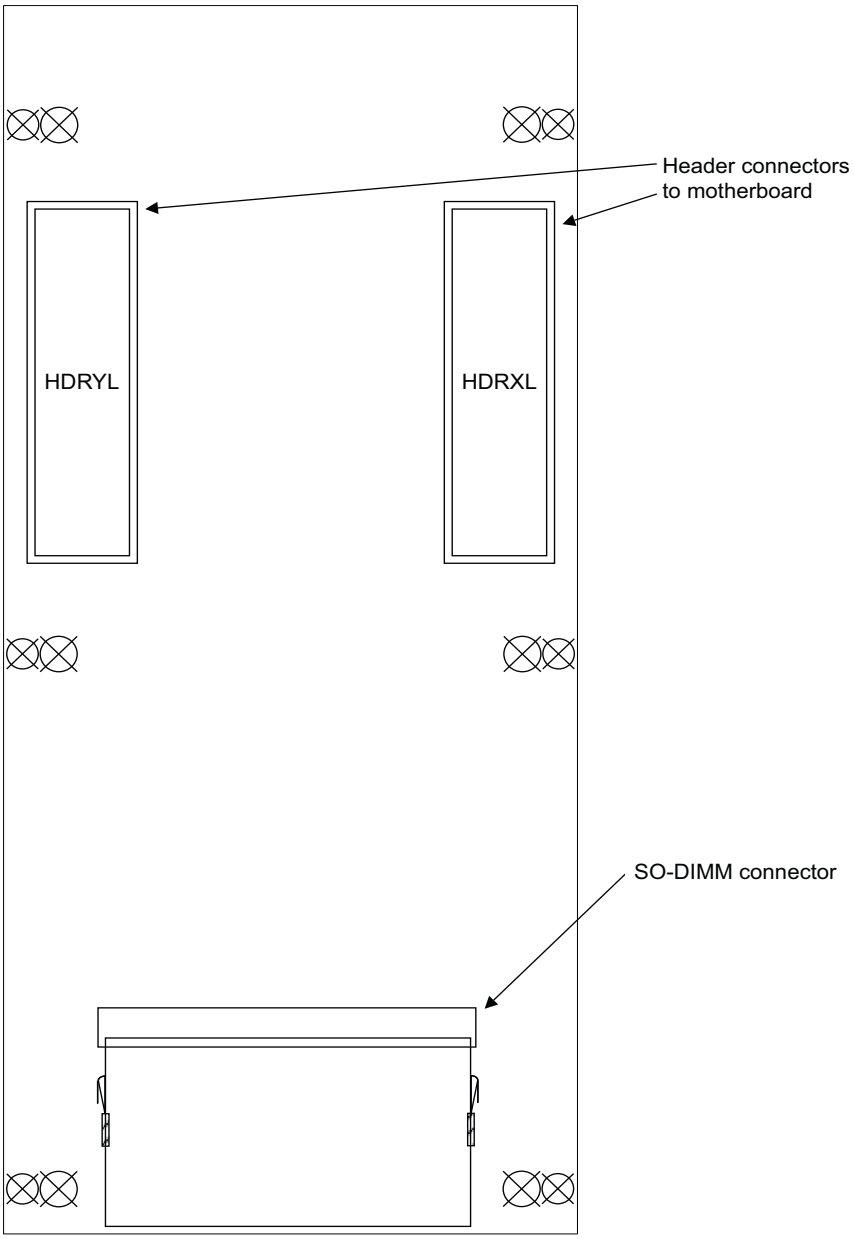


Figure 1-2 Daughterboard layout, bottom

Note

The bottom side of the daughterboard is the side that connects to the motherboard.

Chapter 2
Hardware Description

This chapter describes the LogicTile Express 13MG daughterboard hardware. It contains the following sections:

2.1 Overview of the daughterboard hardware

The hardware infrastructure supports system expansion and a number of debug interfaces. Figure 2-1 shows the high-level hardware infrastructure. For information on the connector signals to these additional interfaces, see Appendix A *Signal Descriptions*.

Note

The configuration images loaded into the two FPGAs at power-up define the functionality of the daughterboard. Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, provided by ARM, implements an example AMBA 3.0 system using the daughterboard.

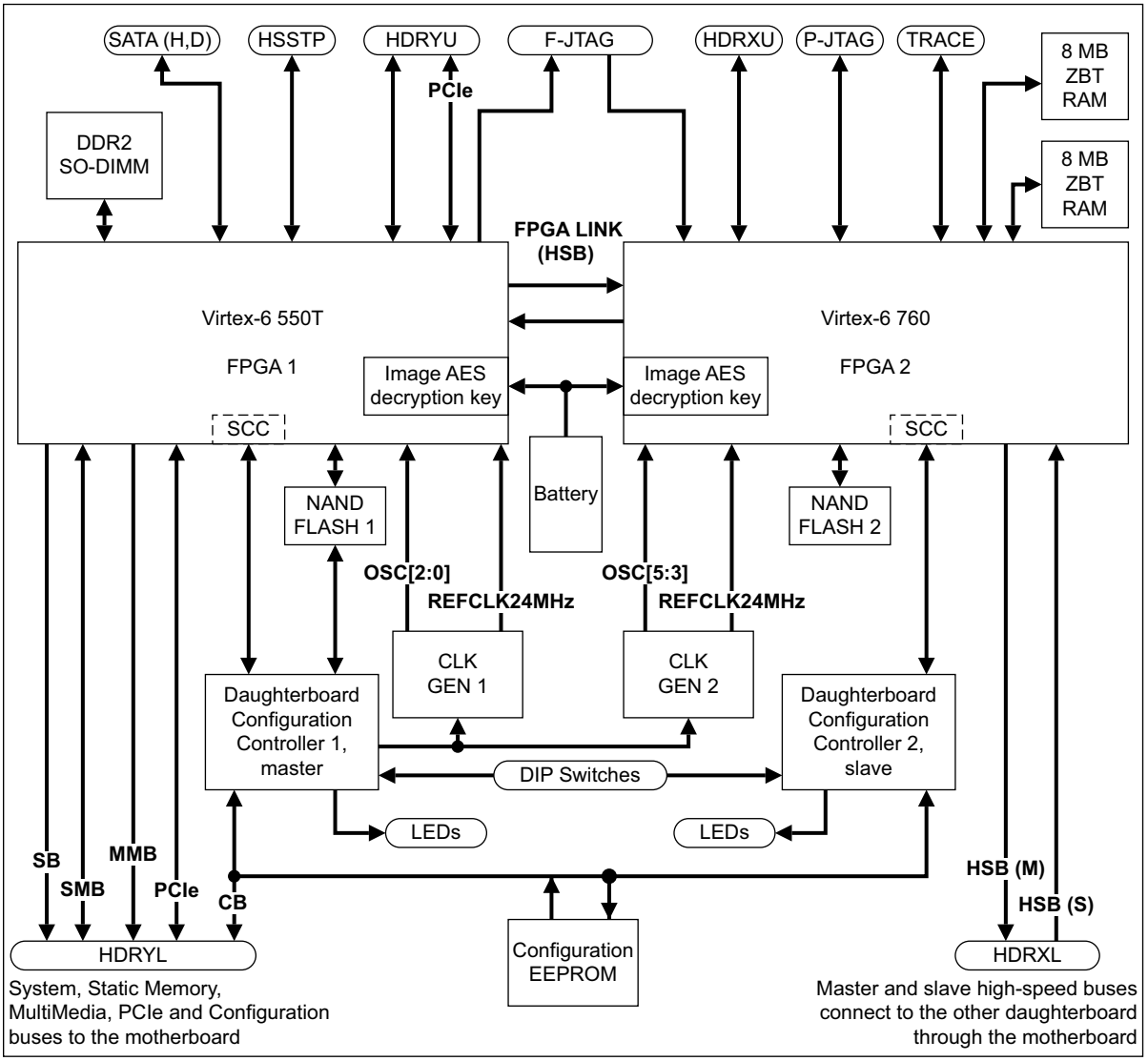


Figure 2-1 Hardware infrastructure

The hardware infrastructure of the daughterboard comprises:

- Two Xilinx Virtex-6 FPGAs:
  - XC6VLX550T, FPGA 1, 5.5 million gates, Gigabit transceiver connection to SATA and HSSTP connectors, speed grade -1.

  - XC6VLX760, FPGA 2, 7.6 million gates, speed-grade -1.
- Two NAND Flash memories, one for each FPGA, used to store FPGA images.
- A configuration EEPROM that is used to store the board *Hardware Board International* (HBI) number and names of the current FPGA images.
- Two local Daughterboard Configuration Controllers, one for each FPGA, whose purpose is to:
  - Set the oscillator frequencies.
  - Set and monitor the power supply voltages.
  - Load the FPGA images.
  - Transfer SCC register values.
- 16MB of on-board ZBT RAM:
  - Two independent banks of 8MB RAM that is driven by FPGA 2.
- SO-DIMM memory connector:
  - 4GB of external DDR2 RAM fitted in the SO-DIMM connector that is driven by FPGA 1.
- One header connector, HDRXL, on the bottom side of the board for routing *High-Speed Buses* (HSBs) from FPGA 2 to the other daughterboard site on the motherboard:
  - One High-Speed Bus Master, M, interface implemented on FPGA 2.
  - One High-Speed Bus Slave, S, interface implemented on FPGA 2.
  - *Low Voltage Differential Signaling* (LVDS) support, 160 pairs.
  - 20 single-ended signals.
- One header connector, HDRYL, for routing buses to the motherboard:
  - *MultiMedia Bus* (MMB).
  - *PCI-Express Bus* (PCIe).
  - *System Bus* (SB).
  - *Static Memory Bus* (SMB).
  - *Configuration Bus* (CB).
- FPGA LINK:
  - An HSB link between the two FPGAs.
  - A Master, M, interface and a HSB slave, S, implemented on each FPGA.
  - LVDS support, 292 single-ended signals that you can configure as up to 146 pairs.
- Two header connectors, HDRXU and HDRYU, on the top side of the board to support upward expansion:
  - 320 single-ended IO pins that you can configure as up to 160 pairs, LVDS, and 20 single-ended IO only pins available on FPGA 2 that connect to HDRXU.
  - 182 general, single-ended, IO pins available on FPGA 1 that connect to HDRYU.
- *Serial Advanced Technology Attachment* (SATA) connectors:
  - One Host, H, connector.
  - One Device, D, connector.
  - Two transmit and two receive lanes in each direction.

- PCI-Express Bus, PCIe:
  - PCIe endpoint capability a maximum 8 lanes upwards and downwards.
- Debug interfaces:
  - P-JTAG port for *RealView*® ICE (RVI) or other compatible third-party debuggers.
  - *Integrated Logic Analyzer* (ILA) F-JTAG port for *ChipScope*, for example.
  - Two trace ports supporting up to 32-bit trace.
  - *High Speed Serial Trace Port* (HSSTP) for prototyping of high-speed trace.
- Two green FPGA DONE_LEDs, one for each FPGA indicating *FPGA configured*.
- Two red OverTemp LEDs, one for each FPGA.
- 18 green general purpose user LEDs, one LED connected directly to each FPGA, and eight LEDs connected to each Daughterboard Configuration Controller.
- Eight general-purpose *Dual In-Line Package* (DIP) switches that are connected to both Daughterboard Configuration Controllers.
- A battery to provide power to both FPGAs, to store FPGA image AES decryption keys.
- Six on-board programmable oscillators:
  - Three input to FPGA 1.
  - Three input to FPGA 2.

For more information, see *System interconnect* on page 2-5.

2.2 System interconnect

This section describes the system interconnect between the LogicTile Express 13MG daughterboard, the Motherboard Express (V2M-P1) and a CoreTile Express daughterboard fitted in site 1 of the V2M-P1 motherboard.

It contains the following subsections:

2.2.1 Overview of system interconnect

Figure 2-2 on page 2-6 shows a typical system interconnect.

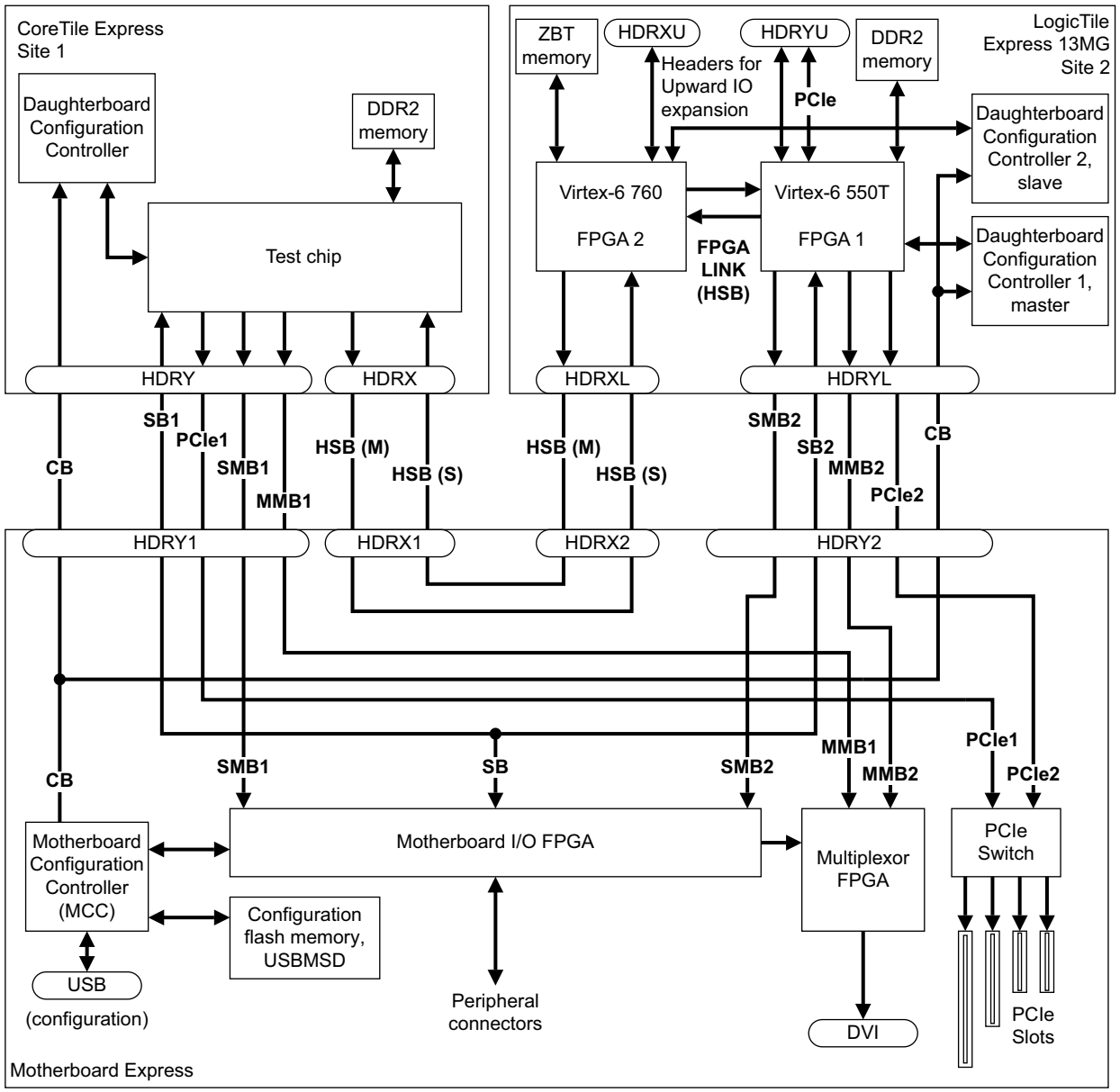


Figure 2-2 System interconnect

The signals on the daughterboard are routed to the motherboard over two header connectors, HDRXL and HDRYL. For more information on the motherboard signals, see Chapter 2 *Hardware Description* of the *ARM® Motherboard Express µATX Technical Reference Manual*.

Note

The V2M-P1 motherboard supports a *root complex* either on the daughterboard in Site 1 or on the daughterboard in Site 2. You select which site contains the *root complex* by editing the `config.txt` file.

Note

ARM recommends that you fit LogicTile Express daughterboards, including the LogicTileExpress 20MG, V2F-1XV7, daughterboard, in site 2, and that you fit CoreTile Express daughterboards in site 1.

2.2.2 FPGA bus widths

Figure 2-3 shows the number of signals available to implement the FPGA buses.

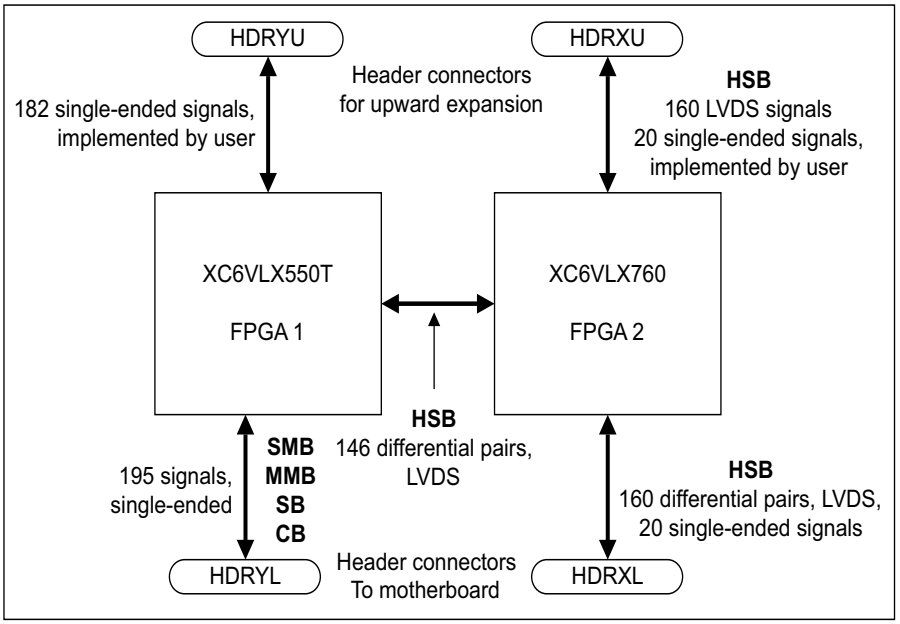


Figure 2-3 Available FPGA bus widths

Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, implements the following buses:

- HSB link to the other daughterboard site on the motherboard. See the `an233_760.ucf` constraints file in application note AN233 for a listing of the 160 LVDS pairs (XP-XN) and the 20 single-ended signals available between FPGA 2 and header HDRXL.
- The HSB link between the two FPGAs. See the `an233_550t.ucf` and `an233_760.ucf` constraints files in application note AN233 for a listing of the LVDS pairs, FPGALINK_P/N, on FPGA 1 and FPGA 2. These signals can also be used as discrete IO.
- The *Static Memory Bus*.
- The *MultiMedia Bus*.
- The *System Bus*.
- The *Configuration Bus*.

Application note AN233 does not implement the following buses:

- HSB link upwards to expansion board. You can implement this yourself by using the 160 LVDS pairs, XP_UP/XN_UP, and 20 single-ended signals available between FPGA 2 and header HDRXU. See the `v2f_760.ucf` constraints file in application note AN233, for a listing of these signals.
- Other buses upwards to an expansion board, for example *Static Memory Bus*, *MultiMedia Bus* and *System Bus*. You can implement these buses yourself by using the 182 single-ended signals available between FPGA 1 and header HDRYU. See the `v2f_550t.ucf` constraints file in application note AN233, for a listing of these signals.

Caution

The FPGAs can be damaged if pins configured as outputs are connected together and output different logic levels to each other.

2.2.3 High-speed buses to other daughterboard

The HDRXL header connects one Master, M, and one Slave, S, HSB, one full duplex bus lane, from FPGA 2 to the other daughterboard through dedicated headers on the motherboard. The most common use of this bus lane is to implement multiplexed AXI master and slave interfaces between the daughterboards.

Note

Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, provides an example AXI design implementing external multiplexed AXI master and slave buses at the HDRXL header. See *FPGA bus widths* on page 2-7.

2.2.4 High-speed buses between the FPGAs, FPGA LINK

292 single-ended IO signals are available between FPGA 1 and FPGA 2. You can use these as discrete IO, or you can configure them as up to 146 LVDS pairs. See Figure 2-3 on page 2-7. You can implement a HSB, for example AXI, between the FPGAs. You can implement a Master, M, interface and a Slave, S, interface on each FPGA to form one full duplex bus lane. See *FPGA 1 clock domains* on page 2-21 and *FPGA 2 clock domains* on page 2-22.

Note

Application note AN233 implements the HSB link between the FPGAs using the FPGA LINK bus. See *FPGA bus widths* on page 2-7.

2.2.5 Buses for upward expansion

The daughterboard can support bus links from FPGA 1 through upper header HDRYU, and from FPGA 2 through upper header HDRXU to another LogicTile Express 13MG daughterboard or user IO expansion board.

340 single-ended IO signals are available between FPGA 2 and upper header HDRXU. You can configure up to 320 of these signals as 160 LVDS pairs. You can only use the other 20 signals as single-ended IO. You can use these signals to implement a HSB bus, for example AXI, to the upper LogicTile 13MG daughterboard or user IO expansion board.

182 single-ended signals are available between FPGA 1 and upper header HDRYU. You can use these signals to implement other buses, for example, SMB, MMB, or SB, to the upper LogicTile 13MG daughterboard or user IO expansion board.

Note

- Application note AN233 does not implement these links but you can implement them yourself using the 160 LVDS pairs and 20 IO signals available between FPGA 1 and header HDRXU, and the 182 single-ended signals available between FPGA 1 and header HDRYU. See *FPGA bus widths* on page 2-7.
- If LogicTile daughterboards are stacked, an external ATX power supply is required.

- LogicTile Express 3MG, V2F-1XV5, boards are not stackable on top of LogicTile Express 13MG, V2F-2XV6, boards because the two boards use different Daughterboard Configuration Controller addressing schemes.
- ARM recommends a maximum stack of two LogicTile Express 13MG boards, and two boards per motherboard site, to enable the use of a common synchronous clock. See *Distribution of global clocks to stacked daughterboards* on page 2-23.

2.2.6 *Static Memory Bus* (SMB)

This connects to FPGA 1. The daughterboard uses the Static Memory Bus for peripheral and memory accesses to the motherboard. This is the minimum bus implementation required to enable the daughterboards to boot and run applications.

2.2.7 *MultiMedia Bus* (MMB)

This connects to FPGA 1. The optional *MultiMedia Bus* (MMB) is implemented to enable the daughterboard to drive audio and video data. The MMB consists of a video bus and I2S and S/PDIF audio buses. This enables the daughterboard to drive up to 1080p or UXGA video and audio formats from stereo to 8-channel surround sound.

2.2.8 *System Bus* (SB)

This connects to FPGA 1. The System Bus carries interrupt and DMA signals between the daughterboards and motherboard.

2.2.9 *Configuration Bus* (CB)

This connects the two Daughterboard Configuration Controllers to the motherboard MCC. The *Configuration Bus* (CB) is used to control the power and reset sequence of the daughterboard and to load or update the images in the FPGAs. The CB also enables SCC register transfers at power-up and during run time. See *FPGA configuration and initialization* on page 2-14.

2.2.10 *PCI-Express Bus* (PCIe)

The V2F-2XV6 can implement a *root complex* to connect, through the motherboard PCIe switch, to the PCI Express Gen1 Card slots on the motherboard. The daughterboard supports a maximum of eight lanes downwards to header HDRYL.

The daughterboard can implement an *endpoint* which supports a maximum of eight lanes upwards to header HDRYU.

Figure 2-4 on page 2-10 shows the PCI-Express signals to the headers. Table 2-1 on page 2-11 shows the connectivity between the Gigabit Transceiver (GTX) locations in the FPGA and the PCI Express lanes.

Note

Xilinx supplies the PCIe endpoint and the PCIe root port in the Virtex-6 FPGA as hardblocks. You can implement them using Xilinx tool flow. You can implement a PCIe root complex using a third party IP softblock.

Note

The V2M-P1 motherboard can support a *root complex* either on the daughterboard in Site 1 or the daughterboard in Site 2, but not both. You select which site contains the *root complex* by editing the `config.txt`. By default, the daughterboard in Site 1 is the *root complex*.

The V2M-P1 motherboard tile sites do not support *endpoints* in the daughterboards connected to the switch.

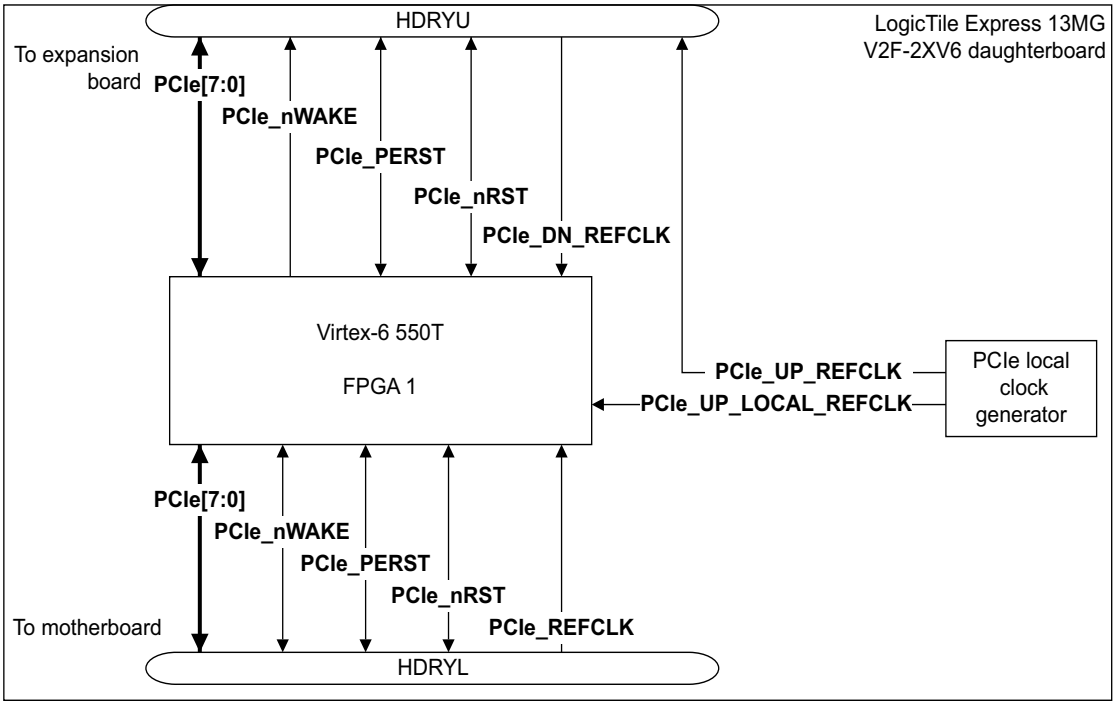


Figure 2-4 PCI express bus connections

Caution

You can configure the sideband signals **PCIe_nWAKE**, **PCIe_PERST**, and **PCIe_nRST** as either inputs or outputs. If you configure them as outputs, they must be set to be open-collector.

Note

- When the daughterboard is fitted to the motherboard, HDRYU is on the upper side of the board facing away from the motherboard, and HDRYL is on the lower side of the board facing towards the motherboard.
- Clocks **PCIe_UP_REFCLK** and **PCIe_UP_LOCAL_REFCLK** are synchronous.

Table 2-1 shows, for the upper header, the connectivity between the *Gigabit Transceiver* (GTX) locations in FPGA 1 and the PCI-Express lanes.

Table 2-1 Upper header PCI-Express Lanes. FPGA 1-GTX connectivity

PCIe lane	GTX location
Lane 0	X0Y15
Lane 1	X0Y14
Lane 2	X0Y13
Lane 3	X0Y12
Lane 4	X0Y11
Lane 5	X0Y10
Lane 6	X0Y9
Lane 7	X0Y8

Table 2-2 shows, for the lower header, the connectivity between the GTX locations in FPGA 1 and the PCI-Express lanes.

Table 2-2 Lower header PCI-Express Lanes. FPGA 1-GTX connectivity

PCIe lane	GTX location
Lane 0	X0Y23
Lane 1	X0Y22
Lane 2	X0Y21
Lane 3	X0Y20
Lane 4	X0Y19
Lane 5	X0Y18
Lane 6	X0Y17
Lane 7	X0Y16

2.2.11 ZBT memory interface

This is implemented in FPGA 2. The ZBT memory interface controls two independent 8MB ZBT SRAM parts. Figure 2-5 on page 2-12 shows the generic FPGA to ZBT SRAM interconnect.

Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, contains an example AXI to ZBT controller, netlist only.

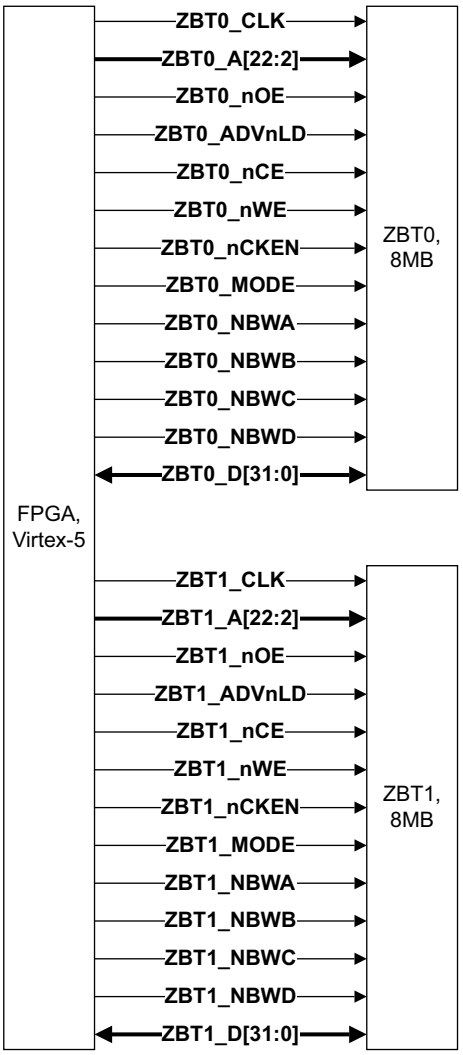


Figure 2-5 Dual ZBT SRAM interface

2.2.12 DDR2 memory interface, SO-DIMM

This is driven by FPGA 1. The SO-DIMM connector supports up to 4GB of 64-bit DDR2 memory expansion. Figure 2-6 on page 2-13 shows the generic FPGA to DDR2 memory interconnect.

Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, contains an example DDR2 controller, netlist only.

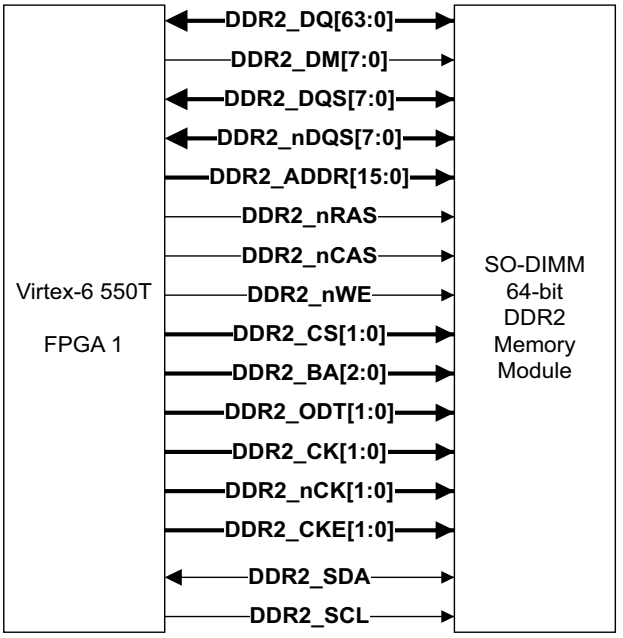


Figure 2-6 DDR2 memory interface

2.2.13 FPGA configuration Flash memory interface

The daughterboard contains two NAND Flash memories. Each Flash memory stores one FPGA image. Each Daughterboard Configuration Controller loads data into its associated Flash memory and initializes the data transfer from the Flash memory to the FPGA.

2.2.14 SATA connectors

Four SATA lanes, two transmit and two receive, from FPGA 1 connect to two SATA connectors. See *SATA connector, J8 and J18* on page A-6.

ARM does not provide an example SATA controller.

2.3 FPGA configuration and initialization

This section describes the FPGA and daughterboard configuration, initialization and resets. It contains the following subsections:

- *Configuration hardware*.
- *FPGA image programming and daughterboard configuration* on page 2-15.
- *Resets* on page 2-15.

2.3.1 Configuration hardware

The daughterboard is fitted with two Xilinx Virtex-6 FPGAs, a XC6VLX550T, FPGA 1, and a XC6VLX760, FPGA 2. Figure 2-7 is shows the FPGAs and other daughterboard components that take part in the daughterboard configuration process.

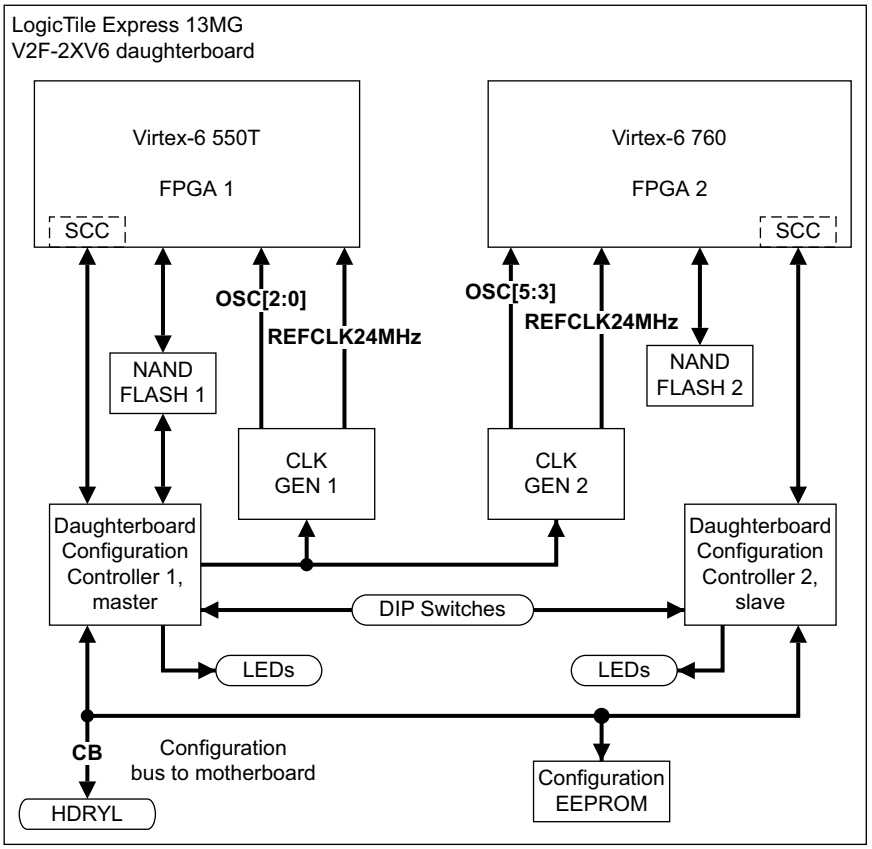


Figure 2-7 Daughterboard FPGA configuration block diagram

2.3.2 FPGA image programming and daughterboard configuration

Configuration is performed during power-up or reset by the *Motherboard Configuration Controller* (MCC) and two Daughterboard Configuration Controllers each with an associated NAND Flash memory. See Figure 2-7 on page 2-14.

Daughterboard Configuration Controller 1, the master Daughterboard Configuration Controller, and NAND Flash 1, configure the 550T FPGA 1. Daughterboard Configuration Controller 1 also sets all the daughterboard oscillator frequencies and FPGA 1 SCC registers using information from the motherboard microSD card, that is a *Universal Serial Bus Mass Storage Device* (USBMSD) card.

Daughterboard Configuration Controller 2, the slave Daughterboard Configuration Controller, and NAND Flash 2, configure the 760 FPGA 2. Daughterboard Configuration Controller 2 also sets the daughterboard FPGA 2 SCC registers.

See *ARM® Versatile™ Express Configuration Technical Reference Manual* and *ARM® Motherboard Express (µATX)* or *ARM® Programmer Module (V2M-CP1)* for information on how to configure the V2F-2XV6 daughterboard using the configuration files on the motherboard.

The V2F-2XV6 provides a DONE_LED for each FPGA to indicate when configuration is complete.

Caution

ARM recommends that you use the configuration files for all system configuration. *SCC register descriptions* on page 3-5, however, describes registers that directly modify the FPGA configuration.

Note

When external power is not present, a battery supplies power to part of the FPGAs that is used to store an AES decryption key. This key is used to enable loading of encrypted images.

2.3.3 Resets

The MCC on the motherboard controls the daughterboard reset signals. Figure 2-8 on page 2-16 shows the reset request signals from the daughterboard, and the reset signals from the motherboard.

Reset requests from the daughterboard can originate in FPGA 1, FPGA 2, or from the P-JTAG connector.

A reset request from the P-JTAG connector can connect to **CB_RSTREQ** through FPGA 2 and Daughterboard Configuration Controller 2.

A reset request from either FPGA can connect to **CB_RSTREQ** through its associated Daughterboard Configuration Controller.

The reset request from the daughterboard results in the motherboard asserting **CB_nRST**. **CB_nPOR** can optionally be asserted by the setting **ASSERTNPOR**, that can be either TRUE or FALSE in the `config.txt` motherboard configuration file. See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for an example `config.txt` file.

Note

Only the **CB_nPOR** and **CB_nRST** signals are driven to the daughterboard FPGAs and Daughterboard Configuration Controllers. **CB_RSTREQ** can be driven from the FPGA through the Daughterboard Configuration Controller to request a cold or warm reset, depending on the motherboard configuration file settings.

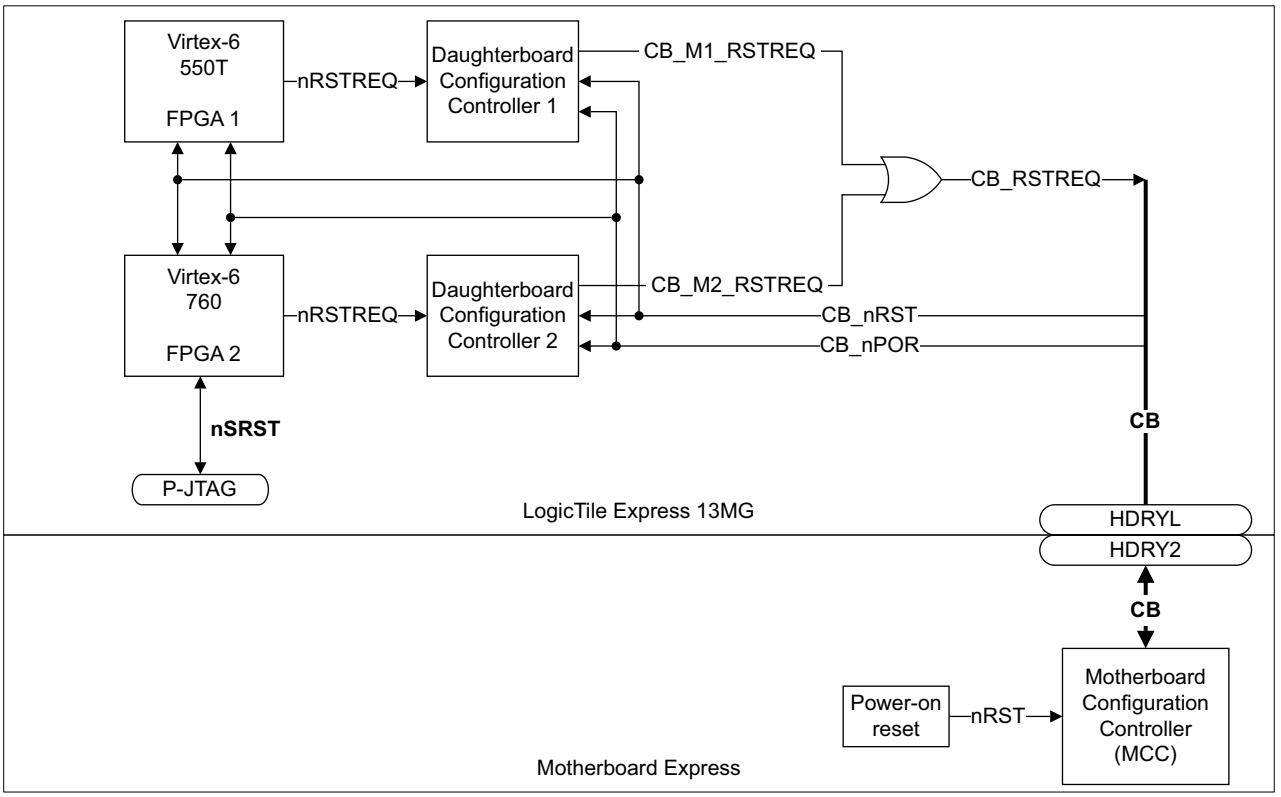


Figure 2-8 Daughterboard resets

Figure 2-9 on page 2-17 shows the basic power-up reset cycle.

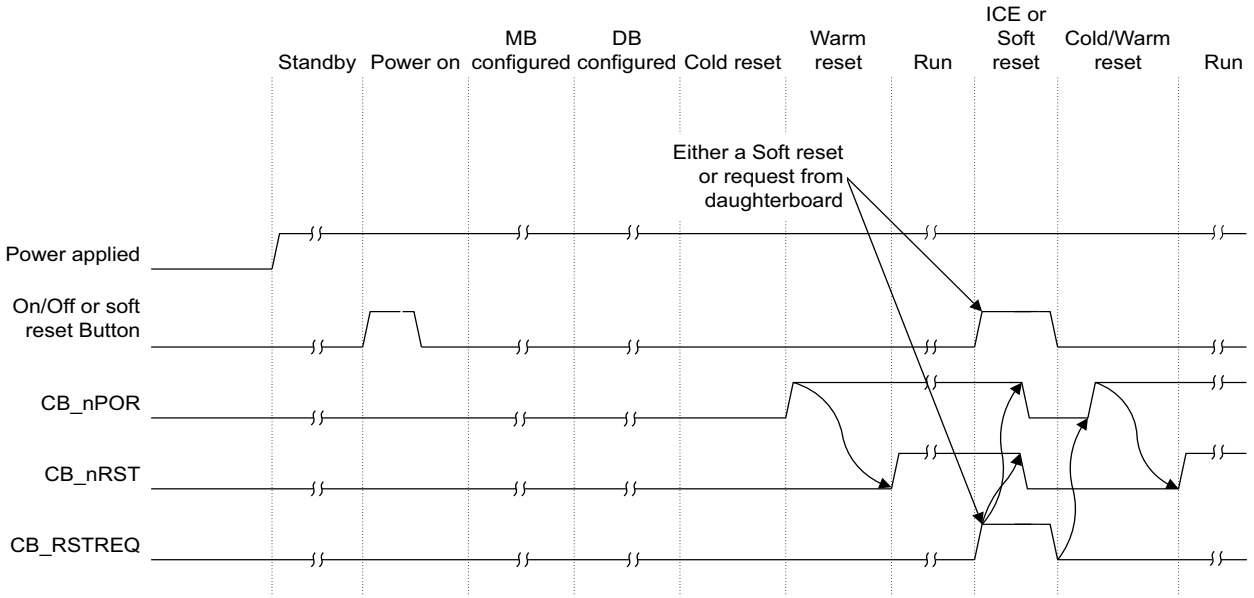


Figure 2-9 Reset timing cycle

2.4 Daughterboard Configuration Controller - FPGA SCC interface

This section describes the interface between the Daughterboard Configuration Controller and the FPGA Serial Configuration Controller (SCC). It contains the following subsections:

- *Overview of Daughterboard Configuration Controller-FPGA SCC interface*.
- *Serial Configuration Controller (SCC)*.

2.4.1 Overview of Daughterboard Configuration Controller-FPGA SCC interface

Each Daughterboard Configuration Controller uses a serial communication channel to receive and transmit information to its associated FPGA on the daughterboard. The FPGA must implement a *Serial Configuration Controller* (SCC) to support these accesses. See Chapter 3 *Programmers Model*. See also Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for an example of a SCC implementation.

The MCC configures the daughterboard SCC registers on power-up with the values that the daughterboard configuration board file defines. You can also read and write to the SCC registers, while the system is running, using the motherboard SYS_CFG register interface.

2.4.2 Serial Configuration Controller (SCC)

The SCC serial interface operates at 0.5MHz. The serial interface is similar to a memory-mapped peripheral because it has an address and a data phase. Figure 2-10 on page 2-19 and Figure 2-11 on page 2-19 show the timing diagrams for write and read operations respectively. The SCC operates a 12-bit address and 32-bit data phase.

The **nCFGRST** output from the Daughterboard Configuration Controller loads the default configuration settings into the FPGA. **CFGLOAD** determines when WRITE DATA is completed, or when READ DATA is expected to be ready. The Daughterboard Configuration Controller provides **CFGCLK** to the FPGA. **CFGWnR** changes depending on the access type.

WRITE DATA is sent *Most Significant Bit* (MSB) first.

READ DATA is received *Least Significant Bit* (LSB) first.

The SCC also has an *Advanced Peripheral Bus* (APB) interface that you can use to access the internal registers.

Note

If the SCC serial interface is not implemented in the FPGA design, ARM recommends that you tie off the **CFGDATAOUT** and **nRSTREQ** signals.

You must tie the **CFGDATAOUT** signal from both FPGAs LOW. These are the **NAND_D[5]** pins on each FPGA.

You must tie the **nRSTREQ** signal from both FPGAs HIGH. These are the **NAND_D[7]** pins on each FPGA.

Figure 2-10 on page 2-19 shows the timing diagram for the write operation.

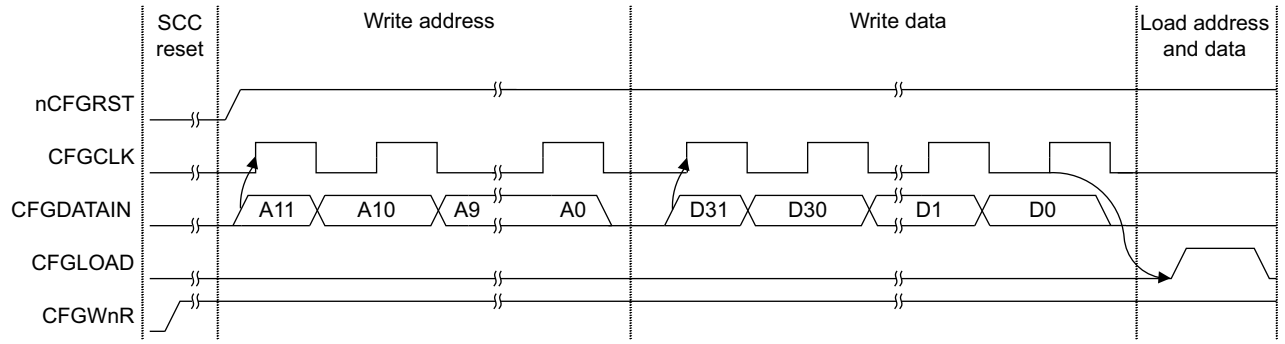


Figure 2-10 Daughterboard Configuration Controller write to SCC

Figure 2-11 shows the timing diagram for the read operation.

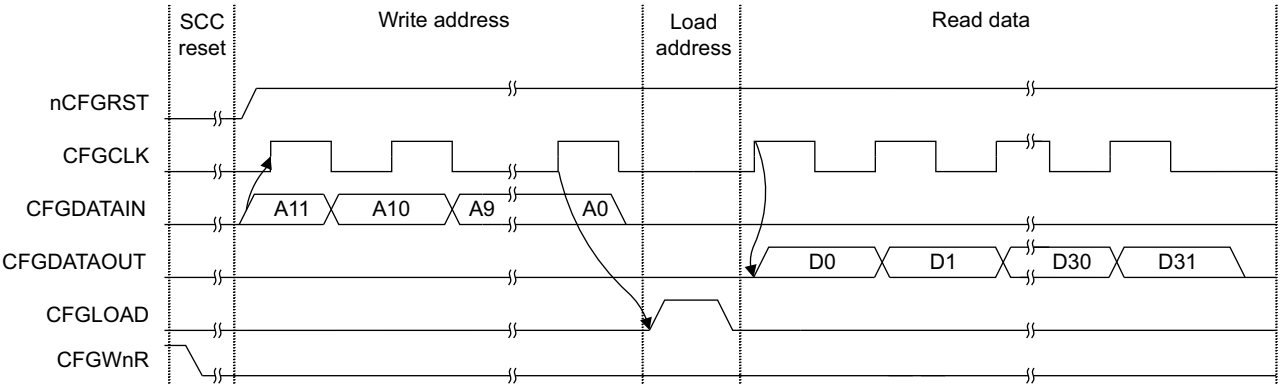


Figure 2-11 Daughterboard Configuration Controller read from SCC

Table 2-3 shows the Daughterboard Configuration Controller AC timing requirements.

Table 2-3 Daughterboard Configuration Controller AC timing requirements for SCC interface

Variable	Time
Daughterboard Configuration Controller output valid time, DCCTov	1µs
Daughterboard Configuration Controller output hold time, DCCToh	1µs
Daughterboard Configuration Controller input setup time, DCCTis	1µs
Daughterboard Configuration Controller input hold time, DCCTih	1µs

2.5 Clocks

This section describes the clocks on the LogicTile Express 13MG daughterboard. It contains the following subsections:

- *Overview of clocks*
- *Clock domains*
- *Global clocks* on page 2-22
- *Distribution of global clocks to stacked daughterboards* on page 2-23

2.5.1 Overview of clocks

The majority of the clocks that the daughterboard uses are generated locally by two on-board clock generators, or within the FPGAs. Each clock generator is associated with one of the FPGAs and contains three oscillators that drive three clocks to its associated FPGA. Figure 2-12 on page 2-21 and Figure 2-13 on page 2-22 show the clock domains of the daughterboard.

The MCC transfers clock settings to Daughterboard Configuration Controller 1 during power-up sequencing using values that the daughterboard configuration files define. Daughterboard Configuration Controller 1 then configures the programmable clock generators.

Table 2-4 shows information on the daughterboard clocks.

Table 2-4 LogicTile Express 13MG daughterboard clocks

Daughterboard clocks	Source	Frequency range	Comment
OSC[2:0]	CLK GEN 1	2MHz-230MHz 1% resolution	Variables OSC0, OSC1 and OSC2 in file f550r0p1.txt configure these daughterboard clocks.
OSC[5:3]	CLK GEN 2	2MHz-230MHz 1% resolution	Variables OSC3, OSC4 and OSC5 in file f550r0p1.txt configure these daughterboard clocks.
SER_CLK	SER CLK GEN	Fixed 150MHz	This is for use if you implement an interface over the SATA connectors.
PCIE_UP_REFCLK **PCIE_REFCLK**	LOCAL PCIE REFCLK	Fixed 100MHz	-
HSSTP_CLK	External clock	-	The LogicTile Express 13MG daughterboard does not generate this clock. See the Xilinx website for information on clock frequencies that the XC6VLX550T FPGA can accept.

See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for information on how to adjust the clock values. Additionally, you can read and write to the daughterboard while the system is running, using the motherboard SYS_CFG register interface.

2.5.2 Clock domains

Figure 2-12 on page 2-21 shows the FPGA 1 clock domains.

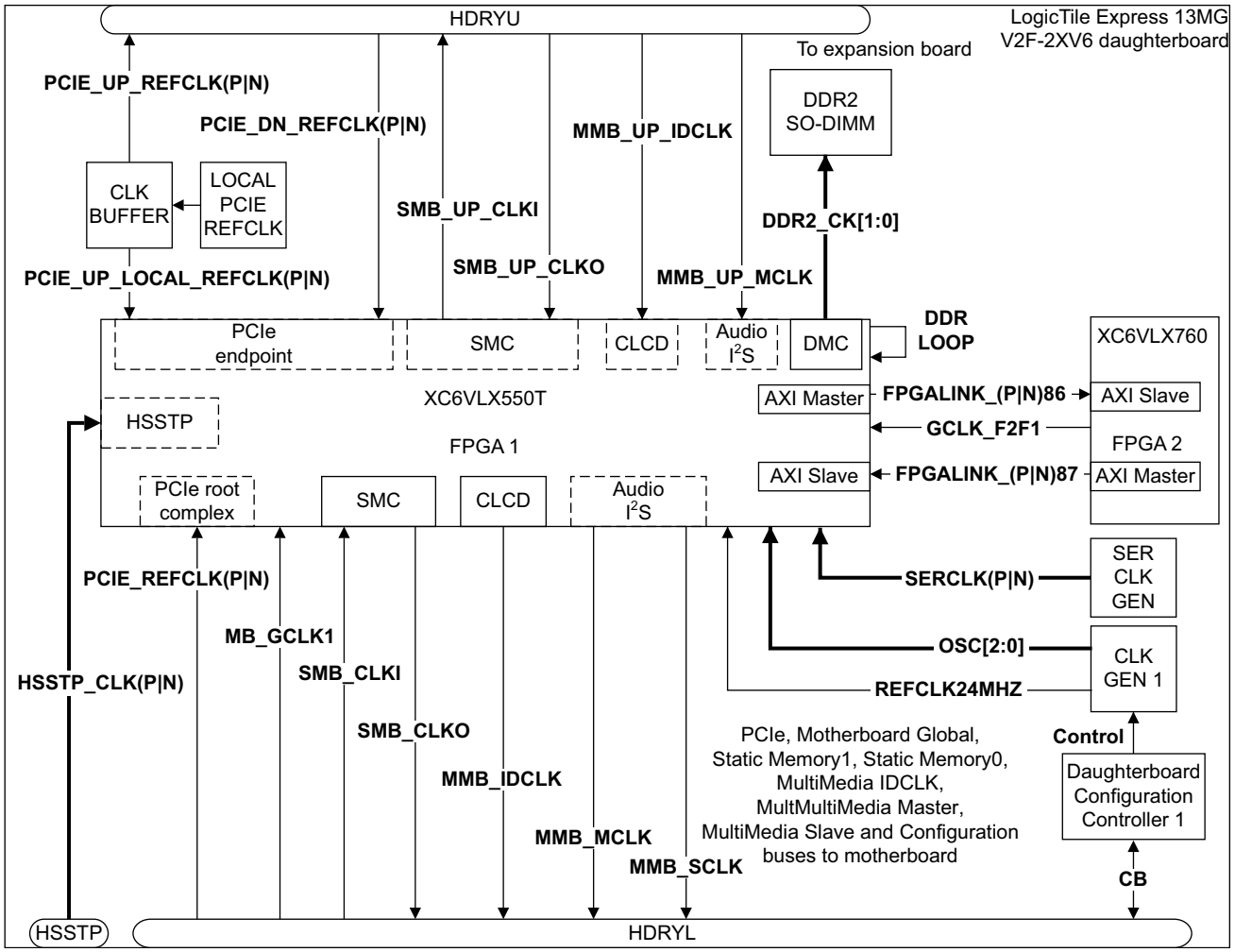


Figure 2-12 FPGA 1 clock domains

Clock loops DDR_LOOP, XU_LOOP, and ZBT_LOOP are available to enable you to use phase-shifted clocks internally in your design while transmitting the non phase-shifted clock externally. See Figure 2-12 and Figure 2-13 on page 2-22. Application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4* contains an example use of phase-shifted clocks.

Note

Figure 2-12 shows the clocks available to implement the functions shown as blocks inside the FPGAs. See the `an233_760.ucf` and `an233_550t.ucf` constraints files supplied in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*. This application note implements the functions shown as solid blocks. It does not supply the functions shown as dashed blocks.

Figure 2-13 on page 2-22 shows the FPGA 2 clock domains.

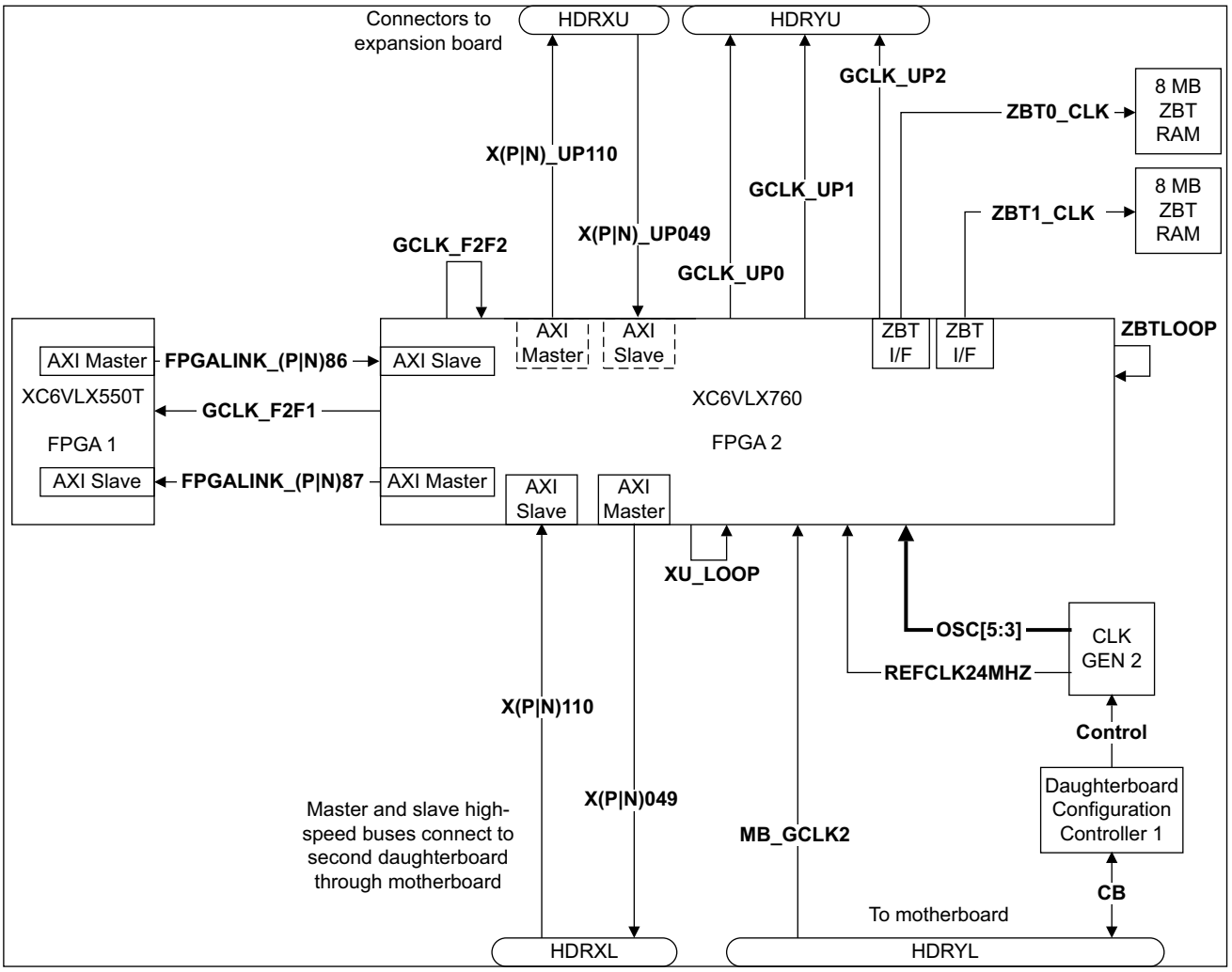


Figure 2-13 FPGA 2 clock domains

Note

Figure 2-13 shows the clocks available to implement the functions shown as blocks inside the FPGAs. See the `an233_760.ucf` and `an233_550t.ucf constraints files` supplied in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*. This application note implements the functions shown as solid blocks. It does not supply the functions shown as dashed blocks.

2.5.3 Global clocks

The global clocks, **GCLK***, on the daughterboard are delay-matched so that they remain synchronous when FPGA 1, FPGA 2, and devices on other boards receive them. See Figure 2-14 on page 2-23. The track lengths of clocks MB_GCLK1 and MB_GCLK2 are delay-matched to length L. **GCLK_F2F2** and **GLCK_F2F1** are delay-matched to length 2L. This enables two LogicTile Express 13MG, V2F-2XV6, daughterboards placed in site 1 and site 2 to receive the synchronous motherboard global clocks. The motherboard drives these clocks to both sites and its clock track lengths are also delay-matched to length L.

Clocks **GCLK_UP0**, **GCLK_UP1**, and **GCLK_UP2** are delay-matched to length L. This enables another daughterboard or expansion board that also has matched clock lengths of L, connected to upper connector HDRYU, to receive the synchronous clocks at the same time as FPGA 1 and FPGA 2 on the LogicTile Express V2F-2XV6 daughterboard.

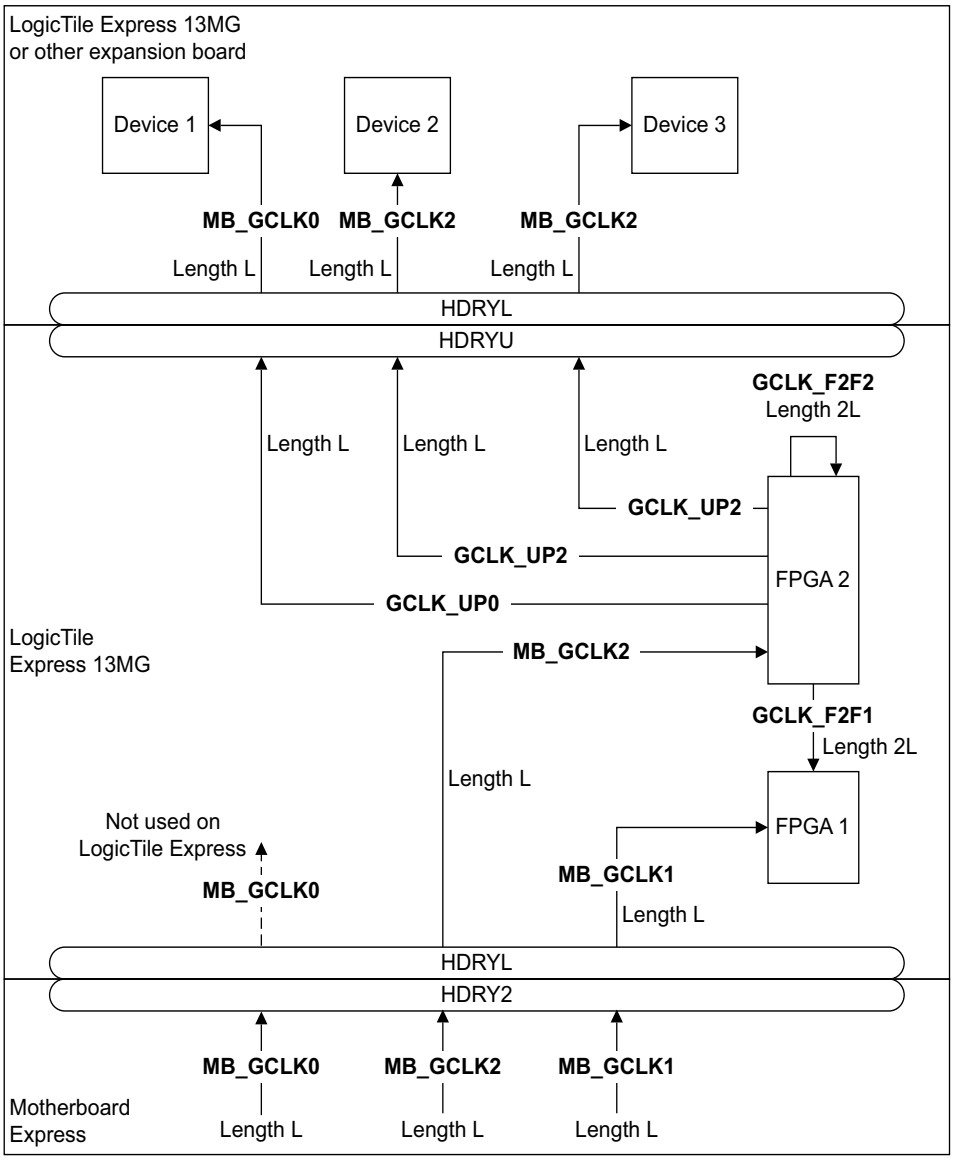


Figure 2-14 Delay-matched clocks

Note

The matched clock length L is 7192 ± 10 mil.

2.5.4 Distribution of global clocks to stacked daughterboards

The V2F-2XV6 13MG daughterboard is designed to enable two daughterboards for each motherboard site to have a common synchronous clock. Figure 2-15 on page 2-24 shows the recommended clocking scheme to distribute a global clock from the motherboard to two stacked daughterboards. You can use this scheme in both motherboard sites to enable four daughterboards to share a common synchronous clock.

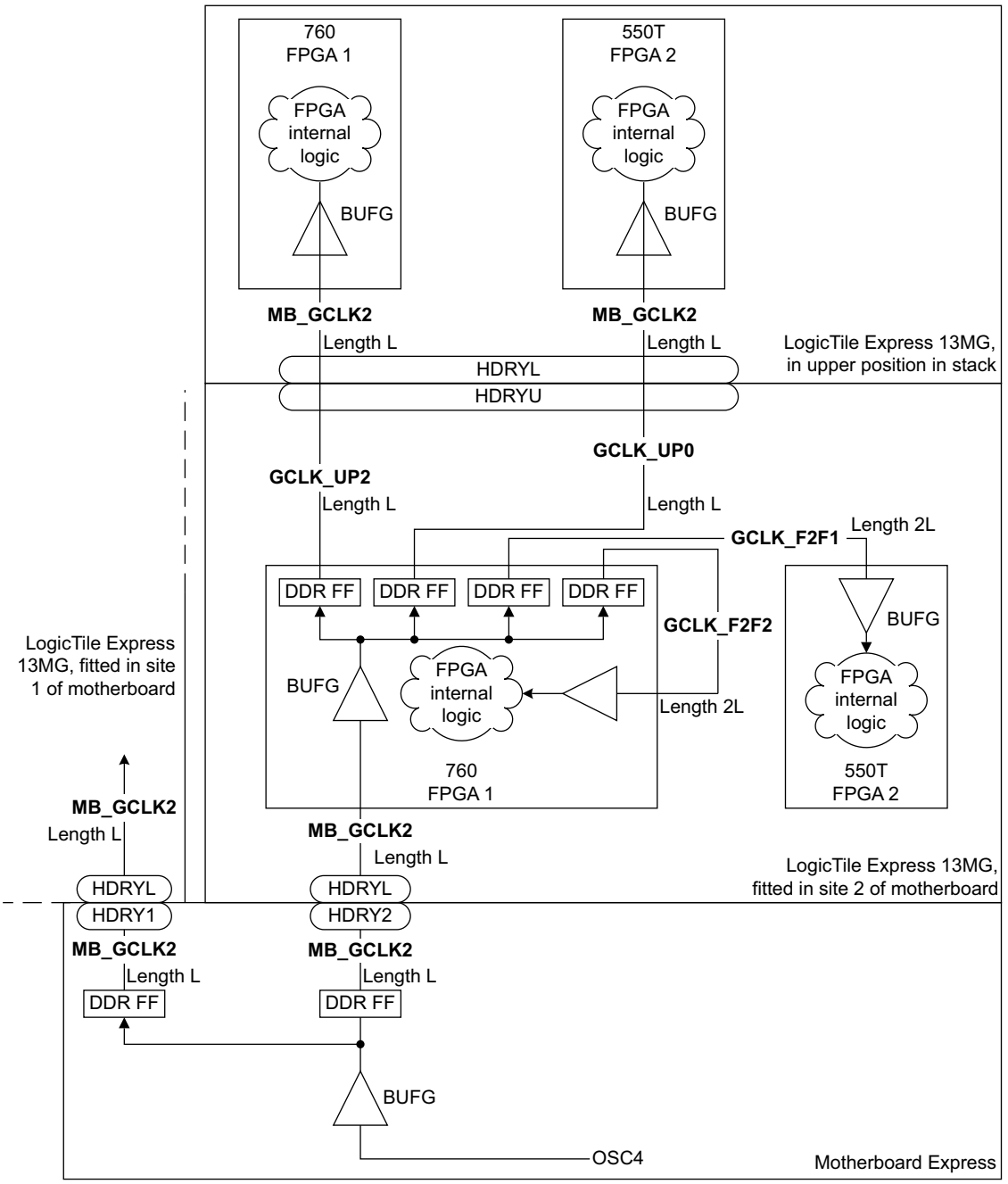


Figure 2-15 Distribution of global clocks to stacked daughterboards

Note

- Figure 2-15 shows the recommended scheme to distribute the global clocks to stacked V2F-2XV6 13MG daughterboards occupying the motherboard sites. Figure 2-15 shows the clocking scheme for site 2, and the same clocking scheme for site 1 is indicated by the partial block on the left of Figure 2-15.
- DDR FF are logic cells and BUFG are buffers provided by Xilinx within the Virtex-6 FPGAs. This clocking scheme uses them to propagate the clocks with identical delays. See the *Virtex-6 FPGA SelectIO Resources User Guide* at the Xilinx web site, http://www.xilinx.com for more information.

2.6 Voltage, temperature, oscillator, and SCC register monitoring

This section describes the monitoring of LogicTile Express 13MG daughterboard operating parameters and the transmission of this information to the V2M-P1 motherboard. It contains the following subsections:

- *Overview of voltage, temperature, oscillator and SCC monitoring.*.
- *Information transmitted by Daughterboard Configuration Controller 1 to the motherboard*.
- *Information transmitted by Daughterboard Configuration Controller 2 to the motherboard* on page 2-26.
- *Daughterboard shutdown because of excessive temperature* on page 2-26.

2.6.1 Overview of voltage, temperature, oscillator and SCC monitoring.

The Daughterboard Configuration Controllers on the daughterboard transmit voltage and temperature measurements and information about the oscillators and SCC registers supported in the two FPGA designs. The Daughterboard Configuration Controllers transmits the information to the motherboard where it can be read from the SYS_CFGCTRL interface.

See the *ARM® Motherboard Express µATX Technical Reference Manual* for more information on the SYS_CFGCTRL registers.

2.6.2 Information transmitted by Daughterboard Configuration Controller 1 to the motherboard

Daughterboard Configuration Controller 1 on the daughterboard transmits voltage measurements, information about the daughterboard oscillators, temperature measurements of FPGA 1, 550T, and FPGA 2, 760, and information about the SCC registers supported in the FPGA 1, 550T, design.

Table 2-5 shows the device numbers for the voltage supplies.

Table 2-5 Device numbers for the voltage supplies

Device	Voltage supply	Default voltage	Description
0	VIO_UP	0.8 +/- 5%	VIO to expansion board above. You can set VIO_UP to any of the voltages shown.
		1.0 +/- 5%	
		1.2 +/- 5%	
		1.5 +/- 5%	
		1.8 +/- 5%	
		2.5 +/- 5%	
1	12	12 +/- 5%	12V from power connector U51.

Table 2-6 shows the device numbers for the daughterboard oscillators.

Table 2-6 Device numbers for oscillator frequencies

Device	Oscillator	Description
0	OSC0	These oscillators connect to FPGA 1, 550T
1	OSC1	
2	OSC2	
3	OSC3	These oscillators connect to FPGA 2, 760
4	OSC4	
5	OSC5	

Table 2-7 shows the device numbers for the FPGA temperature measurements.

Table 2-7 Device numbers for FPGA temperature measurements

Device	Description
0	FPGA 1, 550T, temperature in degrees C, max 80°C
1	FPGA 2, 760, temperature in degrees C, max 80°C

Table 2-8 shows the device numbers for the SCC registers supported in the FPGA 1, 550T, design.

Table 2-8 Devices numbers for the SCC registers supported in the FPGA 1, 550T, design

Device	FPGA 1, 550T, SCC Registers	Description
`0x000` to `0xFFC`	SCC0 to SCC1023	32-bit RW registers, if supported by FPGA 1, 550T, design.

2.6.3 Information transmitted by Daughterboard Configuration Controller 2 to the motherboard

Daughterboard Configuration Controller 2 on the daughterboard transmits information about the SCC registers supported in the FPGA 2 (760) design. Table 2-9 shows the device numbers for the SCC registers.

Table 2-9 Device numbers for the SCC registers

Device	FPGA 2, 760, SCC registers	Description
`0x000` to `0xFFC`	SCC0 to SCC1023	32-bit RW registers, if supported by FPGA 2, 760, design.

2.6.4 Daughterboard shutdown because of excessive temperature

Both FPGAs have an associated red LED that signifies excessive FPGA temperature, D20 for FPGA 1, and D21 for FPGA 2. See Figure 1-1 on page 1-4 for the location of these LEDs on the daughterboard. Each LED illuminates when the internal FPGA temperature exceeds approximately 70°C.

If the internal temperature of the FPGA exceeds 80°C, the MCC powers-down the daughterboard to prevent damage.

2.7 FPGA debug and trace

This section describes the debug and trace interfaces that the LogicTile Express 13MG daughterboard provides. It contains the following subsections:

- *Overview of debug and trace*.
- *F-JTAG*.
- *P-JTAG* on page 2-28.
- *Trace* on page 2-28.
- *HSSTP* on page 2-28.

2.7.1 Overview of debug and trace

Figure 2-16 shows a simplified view of the F-JTAG, P-JTAG, and Trace connections.

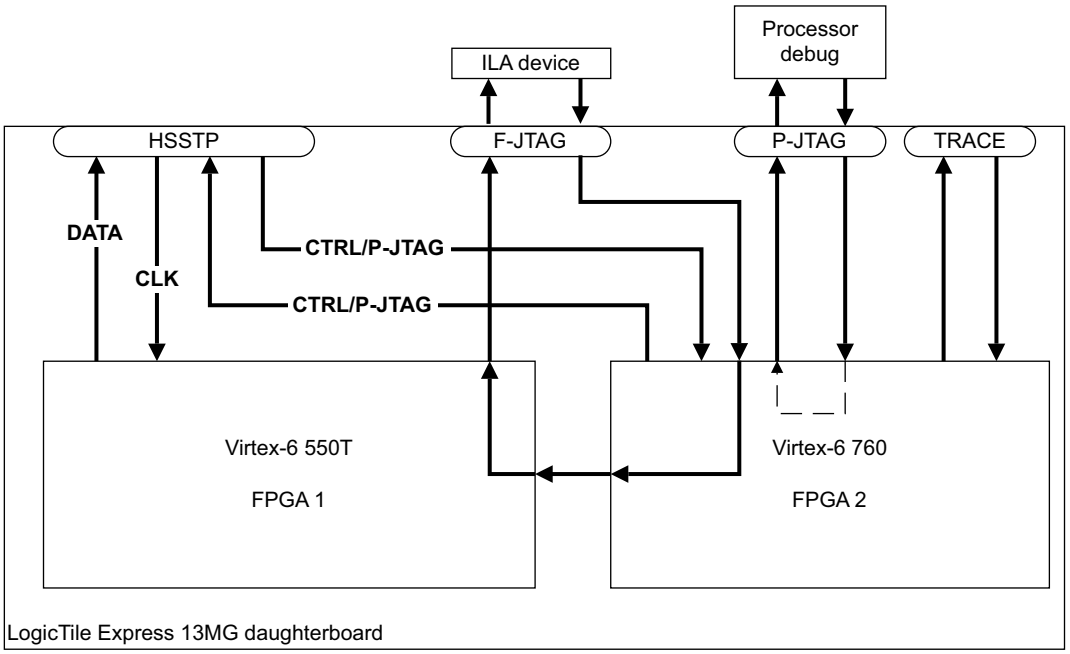


Figure 2-16 Simple JTAG and trace overview

Note

- The ILA device can be any compatible device, for example XChecker or ChipScope.
- The processor debug device can be any compatible debugger, for example *RealView ICE* (RVI).

See also Figure 2-1 on page 2-2 and Figure A-1 on page A-2.

2.7.2 F-JTAG

The F-JTAG (ILA) connector supports FPGA debug. See *F-JTAG (ILA) connector* on page A-5. The *Test Data Input* **TDI** signal is input to FPGA 2 and the *Test Data Output* **TDO** signal is output from FPGA 1. The F-JTAG chain connects to the hard TAP controllers in the FPGAs. See the `v2f_760.ucf`, and `v2f_550t.ucf` constraints files, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

2.7.3 P-JTAG

The P-JTAG connector supports P-JTAG, processor, debug. The use of the P-JTAG chain requires you to connect the P-JTAG signals to a module within FPGA 2 that has a TAP interface and to loop these signals back to form a JTAG chain. See *P-JTAG connector* on page A-5. See also the `v2f_760.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

2.7.4 Trace

Two connectors, Trace Dual and Trace Single, connected to FPGA 2, support 32-bit parallel Trace. See *Trace connectors* on page A-3. See also the `v2f_760.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

2.7.5 HSSTP

A six lane HSSTP connector, connected to FPGA 1 and FPGA 2, also supports Trace. See *HSSTP connector* on page A-7. See also the `v2f_550t.ucf` and `v2f_760.ucf` constraints files, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

2.8 Minimum design settings for daughterboard operation

The minimum RTL in both LogicTile Express FPGAs to operate correctly involves:

- Setting the **SMB_CLKO** output to the inactive LOW state.
- Setting the SMB chip select to the inactive HIGH state.
- Setting **CFGDATAOUT** to the inactive LOW state.
- Setting **nRSTREQ** to the inactive HIGH state.

1. Set the **SMB_CLKO** signal to the inactive LOW state as follows:

   Tie **SMB_CLKO** to `b0`.

   Note

   This stops data being clocked to the IOFPGA on the motherboard.

2. Set the SMB chip select to the inactive HIGH state as follows:

   Tie the chip selects **SMB_nCS** to `b11111111`.

   Note

   This stops static memory access to the motherboard.

3. Set the **CFGATAOUT** signal to the inactive LOW state as follows:

   Tie **NAND_D[5]** to `b0`, as the note in *Serial Configuration Controller (SCC)* on page 2-18 describes.

   Note

   This informs the Daughterboard Configuration Controller that the V2F-2XV6 daughterboard does not implement any of its features.

4. Set the **nRSTREQ** signal to the inactive HIGH state as follows:

   Tie **NAND_D[7]** to `b1`.

   Note

   This prevents **nRSTREQ** from generating a reset. **nRSTREQ** is usually a system-wide master soft reset signal that is both generated and observed by the JTAG debug box.

Note

ARM recommends that all unused pins be tied to their inactive states.

Chapter 3
Programmers Model

This chapter describes the programmers model. It contains the following sections:

3.1 About this programmers model

The following information applies to the SCC:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or power-on reset.
  - Access type in Table 3-1 on page 3-3 is described as follows:

    RW Read and write.

    RO Read only.

    WO Write only.

3.2 Register summary

Table 3-1 shows the registers in offset order from the base memory address.

Table 3-1 Register summary

Offset	Name	Type	Reset	Width	Description
0x000-0x0FC	DCC_CFGx	RW	0xXXXXXXXX[a]	32	*DCC_CFGx registers* on page 3-5
0x100	DCC_LOCK	RO	0xFFXX000X[b]	32	*DCC_LOCK Register* on page 3-5
0x104	DCC_LED	RO	0x0000000F	32	*DCC_LED Register* on page 3-6
0x108	DCC_SW	RO	0x00000000	32	*DCC_SW Register* on page 3-7
0xFF8	DCC_AID	RO	0xXXXXXXXX[a]	32	*DCC_AID Register* on page 3-7
0xFFC	DCC_ID	RO	0xXXXXXXXX[a]	32	*DCC_ID Register* on page 3-8

a. Where X = unknown at reset.

b. Last X = b000X, either b0000 or b0001.

3.3 Memory map

The images that are loaded into the FPGAs determine the LogicTile Express 13MG memory map. See application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4* for an example.

3.4 SCC register descriptions

The Daughterboard Configuration Controllers write to the SCC registers at power-up with the values that the configuration board file defines. The Daughterboard Configuration Controllers also read the LOCK and ID registers to determine whether the PLLs in the FPGAs are locked, and to determine which FPGA image has been loaded. During run-time, the Daughterboard Configuration Controllers poll the LED and Switch values to ensure that they match the SCC register values. The SCC registers are also available during run-time from the motherboard SYG_CFG register interface.

3.4.1 DCC_CFGx registers

The DCC_CFGx registers characteristics are:

Purpose These registers write the USER configuration value. You can define up to 64 write registers. The register address must be in increments of `0x004` and the data must be 32 bits wide. The MCC reads the daughterboard configuration file during board configuration and writes the register values to the FPGA SCC registers. You must implement the appropriate decoder and logic in the FPGA for these to have any effect.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 13MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-1 shows the bit assignments.

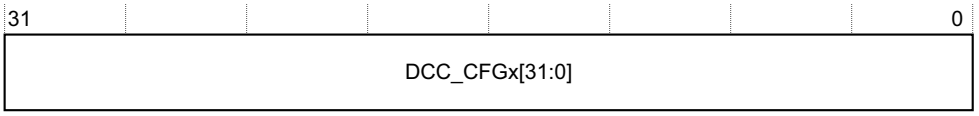


Figure 3-1 DCC_CFGx Registers bit assignments

Table 3-2 shows the bit assignments.

Table 3-2 DCC_CFGx Registers bit assignments

Bits	Name	Function
[31:0]	DCC_CFGx[31:0]	User registers configured during board initialization up from configuration file

Note

You can also update the DCC_CFGx registers during run-time through the motherboard SYS_CFG register interface, motherboard serial port command line interface, or SCC APB interface.

3.4.2 DCC_LOCK Register

The DCC_LOCK Register characteristics are:

Purpose PLL lock status bits from the FPGA.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 13MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-2 shows the bit assignments.

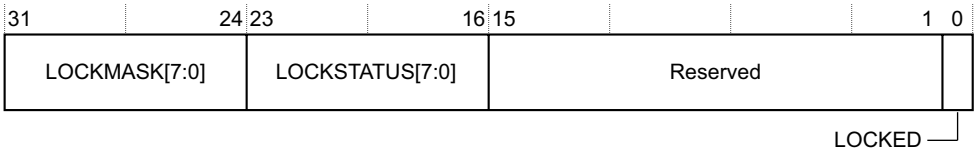


Figure 3-2 DCC_LOCK Register bit assignments

Table 3-3 shows the bit assignments.

Table 3-3 DCC_LOCK Register bit assignments

Bits	Name	Function
[31:24]	LOCK_MASK[7:0]	These bits indicate whether the individual lock bits are masked.
[23:16]	LOCK_STATUS[7:0]	These bits indicate the individual lock status: `b0` Unlocked. `b1` Locked.
[15:1]	-	Reserved.
[0]	LOCKED	This bit indicates whether all unmasked lock bits are locked: `b0` Unlocked. `b1` Locked.

3.4.3 DCC_LED Register

The DCC_LED Register characteristics are:

Purpose Controls the USER LEDs on the daughterboard. The Daughterboard Configuration Controller polls this SCC register from the FPGA and updates the appropriate LEDs.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 13MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-3 shows the bit assignments.

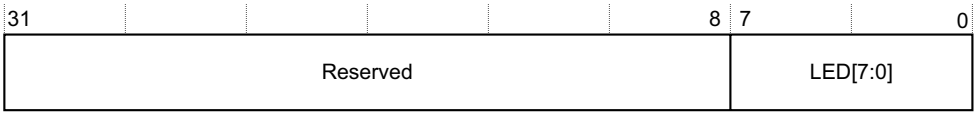


Figure 3-3 DCC_LED Register bit assignments

Table 3-4 shows the bit assignments.

Table 3-4 DCC_LED Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved
[7:0]	LED[7:0]	These bits control the individual USER LEDs

3.4.4 DCC_SW Register

The DCC_SW Register characteristics are:

Purpose Determines the state of the eight user switches on the daughterboard. The Daughterboard Configuration Controller polls the switches and updates this SCC register in the FPGA.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 13MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-4 shows the register bit assignments.

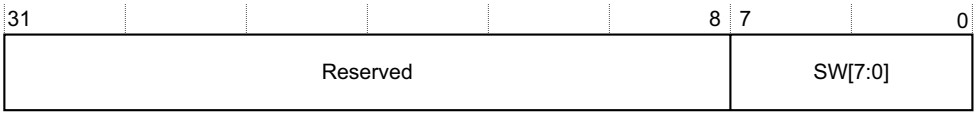


Figure 3-4 DCC_SW Register bit assignments

Table 3-5 shows the bit assignments.

Table 3-5 DCC_SW Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved
[7:0]	SW[7:0]	These bits indicate state of user switches

3.4.5 DCC_AID Register

The DCC_AID Register characteristics are:

Purpose The Daughterboard Configuration Controller reads this information and uses it to determine the number of DCC_CFGx registers and the registers that are supported that can be read from the motherboard SYS-CFG register interface. If this register is not implemented, the Daughterboard Configuration Controller does not support user switches or LEDs, lock, or `user config` commands.

If the FPGA images do not implement SCC interfaces, you must tie the FPGA signal **CFGDATAOUT** to a logic LOW to signal to the Daughterboard Configuration Controller that the FPGA does not transfer data.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 13MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-5 shows the bit assignments.

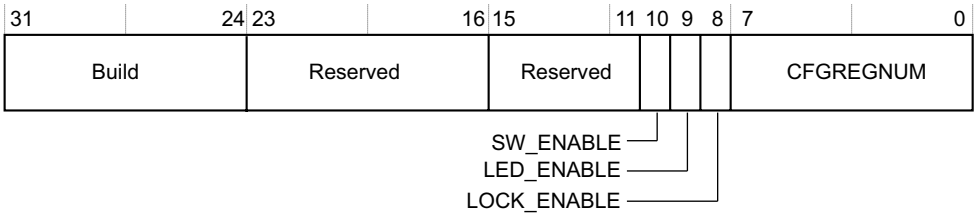


Figure 3-5 DCC_AID Register bit assignments

Table 3-6 shows the bit assignments.

Table 3-6 DCC_AID Register bit assignments

Bits	Name	Function
[31:24]	Build	FPGA build number.
[23:16]	-	Reserved.
[15:11]	-	Reserved.
[10]	SW_ENABLE	This bit indicates whether the DCC_SW_READ command is supported.
[9]	LED_ENABLE	This bit indicates whether the DCC_LED_READ command is supported.
[8]	LOCK_ENABLE	This bit indicates whether the DCC_LOCK_READ command is supported.
[7:0]	CFGREGNUM	These bits indicate the number of user config commands. The maximum supported is 64.

3.4.6 DCC_ID Register

The DCC_ID Register characteristics are:

Purpose The Daughterboard Configuration Controller reads this register and uses it to determine information about the design in the FPGA that you can read through the motherboard SYS_CFG register interface.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 13MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-6 shows the bit assignments.

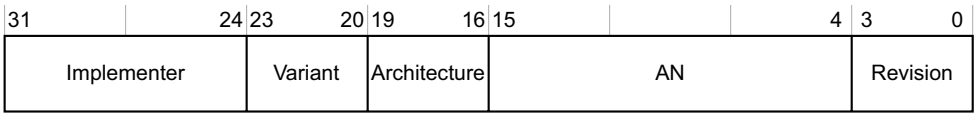


Figure 3-6 DCC_ID Register bit assignments

Table 3-7 shows the bit assignments.

Table 3-7 DCC_ID Register bit assignments

Bits	Name	Function
[31:24]	Implementer	Implementer ID.
[23:20]	Variant	Variant number.
[19:16]	Architecture	Architecture. `0x00` for Application Notes.
[15:4]	AN	Application Note number.
[3:0]	Revision	Revision number.

Appendix A
Signal Descriptions

This chapter describes the signals present at the interface connectors. The on-board connectors are:

A.1 Daughterboard connectors

Figure A-1 shows the connectors fitted to the daughterboard.

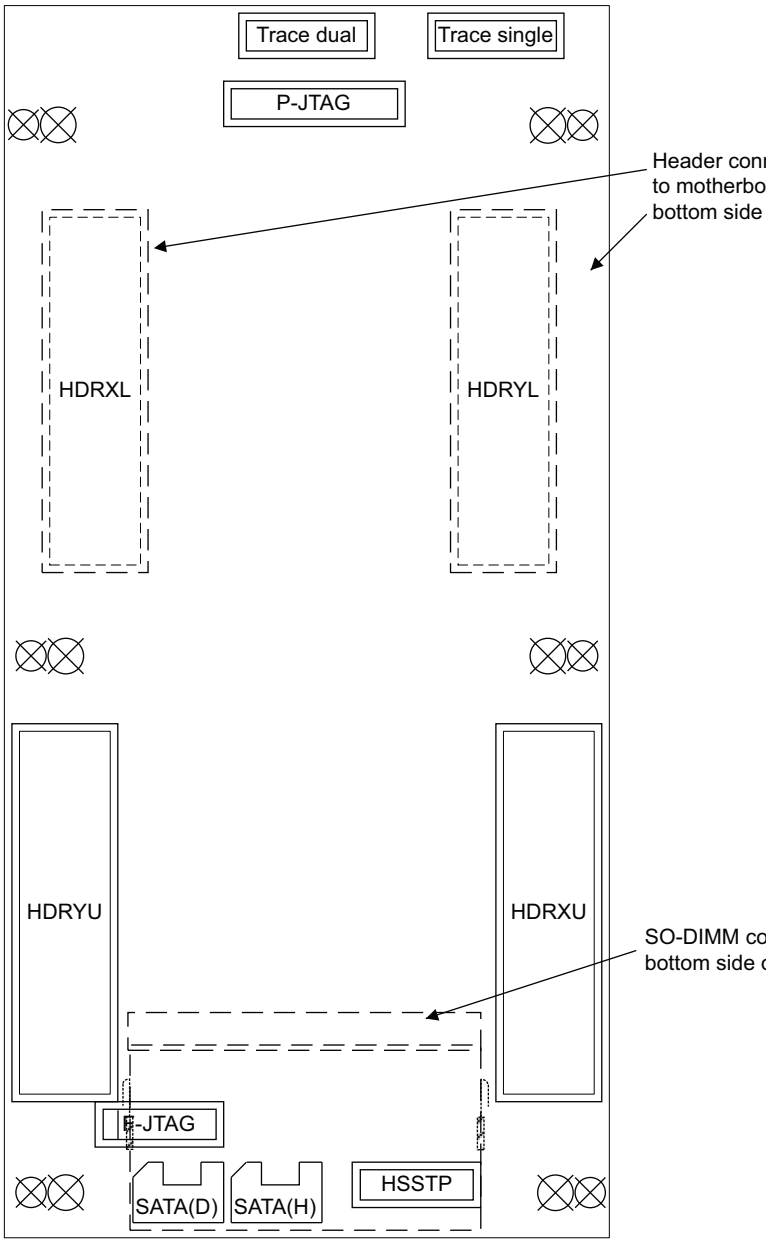


Figure A-1 Daughterboard connectors

A.1.1 Header connectors on lower side of board

There are two high density headers fitted to the underside of the daughterboard. These headers, designated HDRXL, J1, and HDRYL, J2, route the signal and power interconnect to the motherboard and to the other daughterboard site. See the `v2f_760.ucf` and `v2f_550t.ucf` constraints files, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*.

A.1.2 Header connectors on upper side of board

Two high density headers, HDRXU and HDRYU, are fitted to the upper side of the board to support upward expansion. See the `v2f_760.ucf` and `v2f_550t.ucf` constraints files available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*.

The Versatile Express PCIe connector daughterboard, V2C-002, is an example of a board that can be used for upward expansion. See the DVD supplied with the V2F-2XV6 daughterboard for mechanical information.

A.1.3 SO-DIMM connector

The SO-DIMM connector is on the lower side of the board and enables up to 4GB of 64-bit DDR2 memory expansion. It is connected to FPGA 1. You can download the signal list and connector information from the JEDEC web site. See *Other publications* on page ix.

A.1.4 Trace connectors

Two MICTOR trace connectors, labeled *Trace Dual* and *Trace Single*, are connected to FPGA 2. The two connectors used together support 32-bit trace, and the connector labeled *Trace Single*, used alone, supports 16-bit trace. The two trace connectors provide access to a *Trace Port Interface Unit* (TPIU) that can be implemented in FPGA 2.

Note

Examples of trace modules that can be used are RealView ICE and RealView Trace 2.

Figure A-2 shows the MICTOR connector, part number AMP 2-5767004-2.

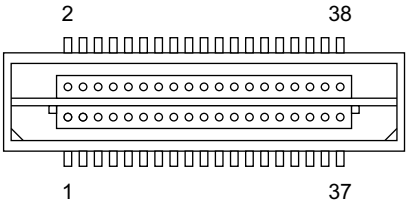


Figure A-2 Trace connector, J9 and J10

Table A-1 lists the trace pin mapping for each *Trace Dual* signal. See the `v2f_760.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-1 Trace dual connector, J10, signal list

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKA**
7	**TRACEDBGRQ**	8	**TRACEDBGACK**
9	**nSRST**	10	**TRACEEXTTRIGX**
11	**TDO**	12	**VTREFA**
13	**RTCK**	14	**VSUPPYLYA**

Table A-1 Trace dual connector, J10, signal list (continued)

Pin	Signal	Pin	Signal
15	**TCK**	16	**TRACEDATA7**
17	**TMS**	18	**TRACEDATA6**
19	**TDI**	20	**TRACEDATA5**
21	**nTRST**	22	**TRACEDATA4**
23	**TRACEDATA15**	24	**TRACEDATA3**
25	**TRACEDATA14**	26	**TRACEDATA2**
27	**TRACEDATA13**	28	**TRACEDATA1**
29	**TRACEDATA12**	30	**GND**
31	**TRACEDATA11**	32	**GND**
33	**TRACEDATA10**	34	**VTREFA** (2V5)
35	**TRACEDATA9**	36	**TRACECTL**
37	**TRACEDATA8**	38	**TRACEDATA0**

Table A-2 lists the Trace pin mapping for each *Trace Single* signal. See the `v2f_760.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-2 Trace single connector, J9, signal list

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKB**
7	Not connected	8	Not connected
9	Not connected	10	Not connected
11	Not connected	12	**VTREF**
13	Not connected	14	Not connected
15	Not connected	16	**TRACEDATA23**
17	Not connected	18	**TRACEDATA22**
19	Not connected	20	**TRACEDATA21**
21	Not connected	22	**TRACEDATA20**
23	**TRACEDATA31**	24	**TRACEDATA19**
25	**TRACEDATA30**	26	**TRACEDATA18**
27	**TRACEDATA29**	28	**TRACEDATA17**
29	**TRACEDATA28**	30	**GND**
31	**TRACEDATA27**	32	**GND**

Table A-2 Trace single connector, J9, signal list (continued)

Pin	Signal	Pin	Signal
33	**TRACEDATA26**	34	**VTREF** (2V5)
35	**TRACEDATA25**	36	**GND**
37	**TRACEDATA24**	38	**TRACEDATA16**

A.1.5 F-JTAG (ILA) connector

The F-JTAG (ILA) connector, J15, is connected to FPGA 1 and FPGA 2. Figure A-3 shows the F-JTAG (ILA) connector. You can use an ILA device such as *ChipScope* to debug designs in the FPGAs.

Note

Pins 2, 4, 6, and 10 on the F-JTAG (ILA) connector have pull-up resistors to 2V5.

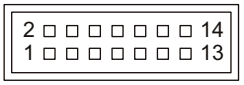


Figure A-3 F-JTAG (ILA) connector, J15

Table A-3 lists the F-JTAG (ILA) pin mapping for each ILA signal. See the `v2f_760.ucf` and `v2f_550t.ucf` constraints files, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-3 F-JTAG (ILA) connector, J15, signal list

Pin	Signal	Pin	Signal
1	**GND**	2	**ILA_2V5**
3	**GND**	4	**ILA_TMS**
5	**GND**	6	**ILA_TCK**
7	**GND**	8	**ILA_TDO**
9	**GND**	10	**ILA_TDI**
11	**GND**	12	Not connected
13	**GND**	14	Not connected

A.1.6 P-JTAG connector

The P-JTAG connector is provided on the daughterboard to enable connection of RealView ICE or a compatible third-party debugger. Figure A-4 on page A-6 shows the P-JTAG connector, J11, that is connected to FPGA 2.

Note

DBGRQ has a pull-down resistor to 0V. **DBGACK** has no pull-up or pull-down resistor. All other signal connections on the P-JTAG connector have pull-up resistors to 2V5.

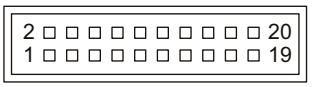


Figure A-4 P-JTAG connector, J11

Table A-4 lists the JTAG pin mapping for each JTAG signal. See the `v2f_760.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-4 P-JTAG connector, J11, signal list

Pin	Signal	Pin	Signal
1	**VIREF**	2	**VSUPPLYA**
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**TMS**	8	**GND**
9	**TCK**	10	**GND**
11	**RTCK**	12	**GND**
13	**TDO**	14	**GND**
15	**nSRST**	16	**GND**
17	**DBGRQ**	18	**GND**
19	**DBGACK**	20	**GND**

A.1.7 SATA connectors

Two SATA connectors on the daughterboard are connected to FPGA 1. Connectivity for two SATA Host, H, and two SATA Device, D, interfaces is provided. Figure A-5 shows the SATA connector.

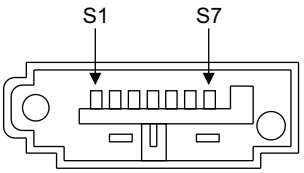


Figure A-5 SATA connector, J8 and J18

Table A-5 on page A-7 lists the SATA Host pin mapping for each SATA signal.

Note

The GTX location for the SATA Host signals is X0Y24. See the `v2f_550t.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-5 SATA Host, J8, signal list

Pin	Signal
S1	**GND**
S2	**SATAH_A_P**
S3	**SATAH_A_N**
S4	**GND**
S5	**SATAH_B_N**
S6	**SATAH_B_P**
S7	**GND**

Table A-6 lists the SATA Device pin mapping for each SATA signal.

Note

The GTX location for the SATA Device signals is X0Y25. See the `v2f_550t.ucf` constraints file, available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-6 SATA Device, J18, signal list

Pin	Signal
S1	**GND**
S2	**SATAD_A_P**
S3	**SATAD_A_N**
S4	**GND**
S5	**SATAD_B_N**
S6	**SATAD_B_P**
S7	**GND**

A.1.8 HSSTP connector

The daughterboard includes the interconnect to implement a *High Speed Serial Trace Port* (HSSTP), connected to FPGA 1 and FPGA 2. The interconnect supports six lanes of LVDS signaling. Figure A-6 on page A-8 shows the HSSTP connector, J7.

Note

Pins 2, 4, and 8 on the HSSTP connector have pull-up resistors to 2V5.

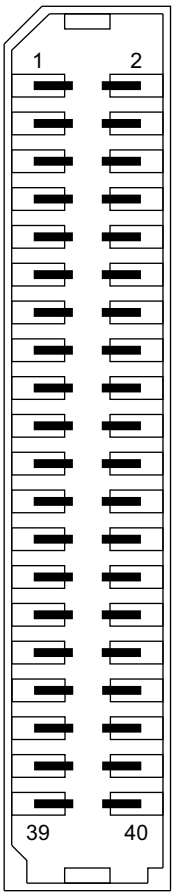


Figure A-6 HSSTP connector, J7

Table A-7 lists the HSSTP pin mapping. See the `v2f_760.ucf` constraints file for trace and debug to FPGA 2 mapping. See the `v2f_550t.ucf` constraints file for serial line to FPGA 1 mapping. Both constraints files are available in application note AN233, *LogicTile Express 13MG example design for a CoreTile Express A9x4*.

Table A-7 HSSTP connector, J10, signal list

Pin	Signal	Pin	Signal
1	**HSSTP_TX4_P**	2	**HSSTP_VTREF**
3	**HSSTP_TX4_N**	4	**HSSTP_TCK**
5	**GND**	6	**GND**
7	**HSSTP_TX2_P**	8	**HSSTP_TMS**
9	**HSSTP_TX2_N**	10	**nTRST**
11	**GND**	12	**GND**
13	**HSSTP_TX0_P**	14	**TDI**
15	**HSSTP_TX0_N**	16	**TDO**
17	**GND**	18	**GND**

Table A-7 HSSTP connector, J10, signal list (continued)

Pin	Signal	Pin	Signal
19	**HSSTP_CLK_P**	20	**nSRST**
21	**HSSTP_CLK_N**	22	**HSSTP_DBGREQ**
23	**GND**	24	**GND**
25	**HSSTP_TX1_P**	26	**HSSTP_DBGACK**
27	**HSSTP_TX1_N**	28	**RTCK**
29	**GND**	30	**GND**
31	**HSSTP_TX3_P**	32	**HSSTP_TRIGIN**
33	**HSSTP_TX3_N**	34	**HSSTP_TRIGOUT**
35	**GND**	36	**GND**
37	**HSSTP_TX5_P**	38	**GND**
39	**HSSTP_TX5_N**	40	**GND**

Table A-8 shows the HSSTP TX FPGA 1-GTX connectivity.

Table A-8 HSSTP TX signal FPGA 1-GTX connectivity

HSSTP signal	GTX location
HSSTP_TX0_P	X0Y29
HSSTP_TX0_N	
HSSTP_TX1_P	X0Y28
HSSTP_TX1_N	
HSSTP_TX2_P	X0Y30
HSSTP_TX2_N	
HSSTP_TX3_P	X0Y27
HSSTP_TX3_N	
HSSTP_TX4_P	X0Y31
HSSTP_TX4_N	
HSSTP_TX5_P	X0Y26
HSSTP_TX5_N	

Appendix B
Specifications

This appendix contains the electrical specification of the daughterboard. It contains the following section:

- *Electrical specification* on page B-2.

B.1 Electrical specification

This section provides information on the current characteristics of the daughterboard.

B.1.1 FPGA current requirements

See the Xilinx web site, http://www.xilinx.com, for software to help you calculate the current requirements for your particular application.

Table B-1 shows the maximum current available to supply each power domain of the FPGAs on the daughterboard and the IO pins on any expansion board supplied through the upper headers, HDRXU and HDRYU.

Table B-1 Available FPGA current

Power domain	Maximum current available	Comment
VCCINT	16A	Supplies the FPGA cores.
VCCAUX	5A	FPGA auxiliary supply voltage.
VIO	4.5A	Current supplied by the motherboard to the daughterboard IO pins that communicate with the motherboard FPGA IO pins.
MGTAVCC	1.8A	Supply for the internal analog circuits of the GTX transceiver on FPGA 1, 550T.
MGTAVTT	1.8A	Analog supply for the transmitter and receiver termination circuits of the GTX transceiver on FPGA 1, 550T.
VIO_UP	9A	Current shared between the IO pins that communicate between FPGA 1 and FPGA 2 and any expansion board supplied through the upper header connectors, HDRXU and HDRYU.

Caution

- It is possible for some FPGA designs to exceed the current and temperature rating of the board. For this reason, you must estimate the power requirements of such designs, using tools such as Xilinx XPE, before implementation.
- The heatsinks supplied on each FPGA have a thermal resistance of 2°C per Watt. The recommended maximum FPGA temperature is 80°C.

Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

Table C-1 Issue A

Change	Location	Affects
No changes, first release	-	-

Table C-2 Differences between Issue A and Issue B

Change	Location	Affects
Minimum design settings for daughterboard operation section added.	*Minimum design settings for daughterboard operation* on page 2-29	All revisions
Changed note text to accommodate new section mentioned above.	*Serial Configuration Controller (SCC)* on page 2-18	All revisions
Changed signal names from **nSRST** to **nRSTREQ**.	Figure 2-8 on page 2-16 *Minimum design settings for daughterboard operation* on page 2-29	All revisions
Added note to say that signal **nRSTREQ** must be tied HIGH when the FPGA design does not support the SCC serial interface.	*Serial Configuration Controller (SCC)* on page 2-18	All revisions
Reference in main text to tying **nSRST** HIGH removed.	*Serial Configuration Controller (SCC)* on page 2-18	All revisions
Changed Signals chapter to Appendix to match other documents in the Versatile Express set.	Appendix A *Signal Descriptions*	All revisions

Table C-3 Differences between Issue B and Issue C

Change	Location	Affects
Glossary removed. Reference and link to *ARM Glossary* inserted.	*Glossary* on page vii	All revisions
Configuration section shortened. Information is now in new document *ARM® Versatile™ Express Configuration Technical Reference Manual.*	*FPGA image programming and daughterboard configuration* on page 2-15	All revisions
New documents added to Additional Reading section of Preface: *ARM® Versatile™ Express Configuration Technical Reference Manual* *ARM® CoreTile Express A5x2 Technical Reference Manual* *ARM® CoreTile Express A15x2 Technical Reference Manual*.	*Additional reading* on page ix	All revisions
Added speed grade to FPGA descriptions.	*About the LogicTile Express 13MG daughterboard* on page 1-3 *Overview of the daughterboard hardware* on page 2-2	All revisions

Table C-4 Differences between Issue C and Issue D

Change	Location	Affects
Added matched clock length L.	*Global clocks* on page 2-22	All revisions

Table C-5 Differences between Issue D and Issue E

Change	Location	Affects
Corrected Trace Dual and Trace single connector labels.	*Trace connectors* on page A-3	All revisions

Table C-6 Differences between Issue E and Issue F

Change	Location	Affects
Added table showing daughterboard clock information.	Table 2-4 on page 2-20	All revisions
Added extra information to clock diagram.	Figure 2-12 on page 2-21	All revisions

Table C-7 Differences between Issue F and Issue G

Change	Location	Affects
Corrected description of PCI-Express system.	*Overview of system interconnect* on page 2-5 *PCI-Express Bus (PCIe)* on page 2-9 Figure 2-12 on page 2-21	All revisions