CoreLink™ MMU-400 Cycle Model
User Guide

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Release Information

The following changes have been made to this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
<th>Confidentiality</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2016</td>
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<td>Initial Restamp Release; r0p0</td>
</tr>
</tbody>
</table>

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http://www.arm.com
## Preface

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Preface

A Cycle Model component is a library developed from ARM® intellectual property (IP) that is generated through Carbon Model Studio™. The Cycle Model then can be used within a virtual platform tool, for example, SoC Designer Plus.

About This Guide

This guide provides all the information needed to configure and use the CoreLink MMU-400 System Memory Management Unit Cycle Model in SoC Designer Plus.

Audience

This guide is intended for experienced hardware and software developers who create components for use with SoC Designer Plus. You should be familiar with the following products and technology:

- SoC Designer Plus
- Hardware design verification
- Verilog or SystemVerilog programming language

Conventions

This guide uses the following conventions:

<table>
<thead>
<tr>
<th>Convention</th>
<th>Description</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>courier</td>
<td>Commands, functions, variables, routines, and code examples that are set apart from ordinary text.</td>
<td><code>sparseMem_t SparseMemCreateNew();</code></td>
</tr>
<tr>
<td>Convention</td>
<td>Description</td>
<td>Example</td>
</tr>
<tr>
<td>------------</td>
<td>-------------</td>
<td>---------</td>
</tr>
<tr>
<td><em>italic</em></td>
<td>New or unusual words or phrases appearing for the first time.</td>
<td><em>Transactors</em> provide the entry and exit points for data ...</td>
</tr>
<tr>
<td><strong>bold</strong></td>
<td>Action that the user performs.</td>
<td>Click <em>Close</em> to close the dialog.</td>
</tr>
<tr>
<td><code>&lt;text&gt;</code></td>
<td>Values that you fill in, or that the system automatically supplies.</td>
<td><code>&lt;platform&gt;/</code> represents the name of various platforms.</td>
</tr>
<tr>
<td><code>[ text ]</code></td>
<td>Square brackets [ ] indicate optional text.</td>
<td><code>$CARBON_HOME/bin/modelstudio [ &lt;filename&gt; ]</code></td>
</tr>
<tr>
<td>`[ text1</td>
<td>text2 ]`</td>
<td>The vertical bar</td>
</tr>
</tbody>
</table>

Also note the following references:

- References to C code implicitly apply to C++ as well.
- File names ending in .cc, .cpp, or .cxx indicate a C++ source file.

**Further reading**

The following publications provide information that relate directly to SoC Designer Plus:

- *SoC Designer Plus Installation Guide*
- *SoC Designer Plus User Guide*
- *SoC Designer Plus Standard Model Library Reference Manual*

The following publications provide reference information about ARM® products:

- *ARM CoreLink MMU-400 System Memory Management Unit Technical Reference Manual*
- *AMBA® Specification*

See [http://infocenter.arm.com/help/index.jsp](http://infocenter.arm.com/help/index.jsp) for access to ARM documentation.

The following publications provide additional information on simulation:

Glossary

AMBA  Advanced Microcontroller Bus Architecture. The ARM open standard on-chip bus specification that describes a strategy for the interconnection and management of functional blocks that make up a System-on-Chip (SoC).

AHB  Advanced High-performance Bus. A bus protocol with a fixed pipeline between address/control and data phases. It only supports a subset of the functionality provided by the AMBA AXI protocol.

APB  Advanced Peripheral Bus. A simpler bus protocol than AXI and AHB. It is designed for use with ancillary or general-purpose peripherals such as timers, interrupt controllers, UARTs, and I/O ports.

AXI  Advanced eXtensible Interface. A bus protocol that is targeted at high performance, high clock frequency system designs and includes a number of features that make it very suitable for high speed sub-micron interconnect.

Cycle Model  A software object created by the Carbon Model Studio (or Carbon compiler) from an RTL design. The Cycle Model contains a cycle- and register-accurate model of the hardware design.

Carbon Model Studio  Graphical tool for generating, validating, and executing hardware-accurate software models. It creates a Cycle Model, and it also takes a Cycle Model as input and generates a component that can be used in SoC Designer Plus, Platform Architect, or Accellera SystemC for simulation.

CASI  ESL API Simulation Interface, is based on the SystemC communication library and manages the interconnection of components and communication between components.

CADI  ESL API Debug Interface, enables reading and writing memory and register values and also provides the interface to external debuggers.

CAPI  ESL API Profiling Interface, enables collecting historical data from a component and displaying the results in various formats.

Component  Building blocks used to create simulated systems. Components are connected together with unidirectional transaction-level or signal-level connections.

ESL  Electronic System Level. A type of design and verification methodology that models the behavior of an entire system using a high-level language such as C or C++.

HDL  Hardware Description Language. A language for formal description of electronic circuits, for example, Verilog.

RTL  Register Transfer Level. A high-level hardware description language (HDL) for defining digital circuits.

SoC Designer  A high-performance, cycle accurate simulation framework which is targeted at System-on-a-Chip hardware and software debug as well as architectural exploration.

SystemC  SystemC is a single, unified design and verification language that enables verification at the system level, independent of any detailed hardware and software implementation, as well as enabling co-verification with RTL design.

Transactor  Transaction adaptors. You add transactors to your component to connect your component directly to transaction level interface ports for your particular platform.
Chapter 1

Using the Cycle Model Component in SoC Designer Plus

This chapter describes the functionality of the MMU-400 Cycle Model and how to use it in SoC Designer Plus. It contains the following sections:

• MMU-400 Memory Management Unit Functionality
• Adding and Configuring the SoC Designer Plus Component
• Available Component ESL Ports
• Setting Component Parameters
• Debug Features
• Available Profiling Data

1.1 MMU-400 Memory Management Unit Functionality

The MMU-400 Cycle Model simulates the ARM® CoreLink™ System MMU-400 Memory Management Unit, which controls address translation, access permissions, memory attribute determination, and checking at a memory system level. The MMU-400 implements the AMBA® AXI3™, AXI4™ and ACE-Lite™ protocols. It supports a single master interface.

For details about the functionality of the hardware that the Cycle Model simulates, refer to the ARM CoreLink MMU-400 System Memory Management Unit Technical Reference Manual.
1.1.1 Hardware Features not Implemented

The following features of the MMU-400 hardware are not implemented in the MMU-400 Cycle Model:

- The register view is not available in SoC Designer Plus.
- The MMU-400 Cycle Model currently has no debug support.
- Hardware and software profiling are not currently supported.

1.2 Adding and Configuring the SoC Designer Plus Component

The following topics briefly describe how to use the component. See the SoC Designer Plus User Guide for more information.

- SoC Designer Plus Component Files
- Adding the Cycle Model to the Component Library
- Adding the Component to the SoC Designer Canvas

1.2.1 SoC Designer Plus Component Files

The component files are the final output from the Carbon Model Studio compile and are the input to SoC Designer Plus. There are two versions of the component; an optimized release version for normal operation, and a debug version.

On Linux the debug version of the component is compiled without optimizations and includes debug symbols for use with gdb. The release version is compiled without debug information and is optimized for performance.

On Windows the debug version of the component is compiled referencing the debug runtime libraries, so it can be linked with the debug version of SoC Designer Plus. The release version is compiled referencing the release runtime library. Both release and debug versions generate debug symbols for use with the Visual C++ debugger on Windows.

The provided component files are listed in Table 1-1:

<table>
<thead>
<tr>
<th>Platform</th>
<th>File Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux</td>
<td>maxlib.lib&lt;component_name&gt;.conf</td>
<td>SoC Designer Plus configuration file</td>
</tr>
<tr>
<td></td>
<td>lib&lt;component_name&gt;.mx.so</td>
<td>SoC Designer Plus component runtime file</td>
</tr>
<tr>
<td></td>
<td>lib&lt;component_name&gt;.mx_DBG.so</td>
<td>SoC Designer Plus component debug file</td>
</tr>
<tr>
<td>Windows</td>
<td>maxlib.lib&lt;component_name&gt;.windows.conf</td>
<td>SoC Designer Plus configuration file</td>
</tr>
<tr>
<td></td>
<td>lib&lt;component_name&gt;.mx.dll</td>
<td>SoC Designer Plus component runtime file</td>
</tr>
<tr>
<td></td>
<td>lib&lt;component_name&gt;.mx_DBG.dll</td>
<td>SoC Designer Plus component debug file</td>
</tr>
</tbody>
</table>

Additionally, this User Guide PDF file is provided with the component.
1.2.2 Adding the Cycle Model to the Component Library

The compiled Cycle Model component is provided as a configuration file (.conf). To make the component available in the Component Window in SoC Designer Canvas, perform the following steps:

1. Launch SoC Designer Canvas.
2. From the File menu, select Preferences.
3. Click on Component Library in the list on the left.
4. Under the Additional Component Configuration Files window, click Add.
5. Browse to the location where the Cycle Model is located and select the component configuration file:
   - maxlib.lib<component_name>.conf (for Linux)
   - maxlib.lib<component_name>.windows.conf (for Windows)
6. Click OK.
7. To save the preferences permanently, click the OK & Save button.

The component is now available from the SoC Designer Plus Component Window.

1.2.3 Adding the Component to the SoC Designer Canvas

Locate the component in the Component Window and drag it out to the Canvas. Note that the presence of certain ports and configuration options depends on the initial configuration of the Cycle Model (for example, ACE_Lite, AXI3, or AXI4).

1.3 Available Component ESL Ports

Table 1-2 describes the MMU-400 Cycle Model ESL ports that are exposed in SoC Designer Plus.

<table>
<thead>
<tr>
<th>ESL Port</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;protocol&gt;_s l</td>
<td>Slave port for the protocol.</td>
<td>Transactor slave</td>
</tr>
<tr>
<td>&lt;protocol&gt;_m l</td>
<td>Master port for the protocol.</td>
<td>Transactor master</td>
</tr>
<tr>
<td>apb_ns</td>
<td>APB NonSecure port</td>
<td>Transactor slave</td>
</tr>
<tr>
<td>apb_s</td>
<td>APB Secure port</td>
<td>Transactor slave</td>
</tr>
<tr>
<td>&lt;protocol&gt;_ptw 2</td>
<td>Page Table Walk bus master port</td>
<td>Transactor master</td>
</tr>
<tr>
<td>bclk</td>
<td>Clock that drives AXI ports &quot;&lt;protocol&gt;_s&quot; and &quot;&lt;protocol&gt;_m&quot;</td>
<td>Input Clock</td>
</tr>
<tr>
<td>bresetn</td>
<td>Reset for AXI ports &quot;&lt;protocol&gt;_s&quot; and &quot;&lt;protocol&gt;_m&quot;</td>
<td>Signal Slave</td>
</tr>
<tr>
<td>cclk</td>
<td>Input clock that drives ports &quot;*_ptw&quot;, &quot;apb_s&quot;, apb_ns&quot;</td>
<td>Input Clock</td>
</tr>
</tbody>
</table>
1.4 Setting Component Parameters

You can change the settings of all the component parameters in SoC Designer Canvas, and of some of the parameters in SoC Designer Simulator. To modify the component’s parameters:

1. In the Canvas, right-click on the component and select **Edit Parameters...**. You can also double-click the component. The **Edit Parameters** dialog box appears.

2. In the Parameters window, double-click the **Value field** of the parameter that you want to modify.

3. If it is a text field, type a new value in the **Value field**. If a menu choice is offered, select the desired option. The parameters are described in Table 1-3.

Note that the availability of certain parameters is dependent on your Cycle Model configuration.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Allowed Values</th>
<th>Default Value</th>
<th>Init/Runtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>Align Waveforms</td>
<td>When set to true, waveforms dumped by the component are aligned with the SoC Designer simulation time. The reset sequence, however, is not included in the dumped data. When set to false, the reset sequence is dumped to the waveform data, however, the component time is not aligned with SoC Designer time.</td>
<td>True, False</td>
<td>True</td>
<td>Init</td>
</tr>
<tr>
<td>apb_ns Base Address</td>
<td>Base address of address region 0.</td>
<td>Integer</td>
<td>0</td>
<td>Init</td>
</tr>
<tr>
<td>apb_ns Enable Debug Messages</td>
<td>Enable debug messages.</td>
<td>Bool</td>
<td>False</td>
<td>Runtime</td>
</tr>
<tr>
<td>apb_ns Size</td>
<td>Size of address region 0.</td>
<td>Integer</td>
<td>-</td>
<td>Init</td>
</tr>
<tr>
<td>apb_s Base Address</td>
<td>Base address of address region 0.</td>
<td>Integer</td>
<td>0</td>
<td>Init</td>
</tr>
<tr>
<td>apb_s Enable Debug Messages</td>
<td>Enable debug messages.</td>
<td>Bool</td>
<td>False</td>
<td>Runtime</td>
</tr>
<tr>
<td>apb_s Size</td>
<td>Size of address region 0.</td>
<td>Integer</td>
<td>-</td>
<td>Init</td>
</tr>
</tbody>
</table>
Table 1-3 Component Parameters (continued)

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Allowed Values</th>
<th>Default Value</th>
<th>Init/ Runtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>CarbonDB Path</td>
<td>Sets the directory path to the database file.</td>
<td>Not used</td>
<td>Empty</td>
<td>n/a</td>
</tr>
<tr>
<td>Dump Waveforms</td>
<td>Whether SoC Designer dumps waveforms for this component.</td>
<td>True, False</td>
<td>False</td>
<td>Init</td>
</tr>
<tr>
<td>Enable Debug Messages</td>
<td>Determines whether debug messages are logged for the component.</td>
<td>True, False</td>
<td>False</td>
<td>Init</td>
</tr>
<tr>
<td>&lt;protocol&gt;_m Enable Debug Messages&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Enable debug messages.</td>
<td>True, False</td>
<td>False</td>
<td>Runtime</td>
</tr>
<tr>
<td>&lt;protocol&gt;_m Protocol Variant&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Protocol Variant for transactor.</td>
<td>String</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>&lt;protocol&gt;_ptw Enable Debug Messages&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Enable debug messages.</td>
<td>True, False</td>
<td>False</td>
<td>Runtime</td>
</tr>
<tr>
<td>&lt;protocol&gt;_ptw Protocol Variant&lt;sup&gt;2&lt;/sup&gt;</td>
<td>Protocol Variant for transactor.</td>
<td>String</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>&lt;protocol&gt;_s Enable Debug Messages&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Enable debug messages.</td>
<td>True, False</td>
<td>False</td>
<td>Runtime</td>
</tr>
<tr>
<td>&lt;protocol&gt;_s Protocol Variant&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Protocol Variant for transactor.</td>
<td>String</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>&lt;protocol&gt;_s axi_size&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Size of address region ( n ), where ( n ) is equal to 0, 1, 2, 3, 4, or 5.</td>
<td>Integer</td>
<td>Default for address region 0 = 0x10000000 Default for address regions 1 to 5 = 0</td>
<td>Init</td>
</tr>
<tr>
<td>&lt;protocol&gt; axi_start&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Start address of address region ( n ), where ( n ) is equal to 0, 1, 2, 3, 4, or 5.</td>
<td>Integer</td>
<td>0</td>
<td>Init</td>
</tr>
<tr>
<td>Waveform file</td>
<td>Name of the waveform file.</td>
<td>String</td>
<td>carbon_pl470.vcd</td>
<td>Init</td>
</tr>
<tr>
<td>Waveform format</td>
<td>The format of the waveform dump file.</td>
<td>VCD, FSDB</td>
<td>VCD</td>
<td>Init</td>
</tr>
<tr>
<td>Waveform timescale</td>
<td>Sets the timescale to be used in the waveform.</td>
<td>Set of values in pulldown menu.</td>
<td>1ns</td>
<td>Init</td>
</tr>
</tbody>
</table>

1. Protocol name is configuration-dependent. It may be AXI3, AXI4, or ACE_Lite.
2. Protocol name for _ptw parameters may be AXI (indicates AXI3), AXI4, or ACE_Lite_DVM.

Note: These parameters are obsolete and should be left at their default values.
3. ARM recommends using the Memory Map Editor (MME) in SoC Designer Plus, which provides centralized viewing and management of the memory regions available to the components in a system. For information about migrating existing systems to use the MME, refer to Chapter 9 of the *SoC Designer Plus User Guide*.

1.5 Debug Features

The MMU-400 Cycle Model currently has no debug support.

1.6 Available Profiling Data

Hardware and software profiling are not currently supported.