DWARF for the ARM® 64-bit Architecture (AArch64) with SVE support

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Abstract

This document describes the use of the DWARF debug table format in the Application Binary Interface (ABI) for the ARM 64-bit architecture. It includes support for the Scalable Vector Extension (SVE).

Keywords

DWARF, DWARF 3.0, use of DWARF format

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1 ABOUT THIS DOCUMENT

1.1 Change control

1.1.1 Current status and anticipated changes

This document's status is released for the base specification and is in beta for the SVE support specification. Clarifications, extensions and minor changes should be expected for the base specification, while larger changes are possible but unlikely for the SVE support specification.

1.1.2 Change history

Issue	Date	By	Change
00bet3	16th December 2010	MGD	Beta release.
1.0	22nd May 2013	RE	First public release.
SVEdwf 00bet0	1st June 2016	KW	First beta release including SVE support
SVEdwf 00bet0.1	27th June 2016	KW	The size of the VG register is 64-bit
SVEdwf 00bet1	7th April 2017	KW	Minor typographical corrections

1.2 References

This document refers to, or is referred to by, the following documents.

Ref	External reference or URL	Title
AADWARF	IHI 0057B	DWARF for the ARM 64-bit Architecture (AArch64)
GDWARF	http://www.dwarfstd.org/	DWARF 3.0, the generic debug table format.

1.3 Terms and abbreviations

The *ABI for the ARM 64-bit Architecture* uses the following terms and abbreviations.

Term	Meaning
A32	The instruction set named *ARM* in the ARMv7 architecture; A32 uses 32-bit fixed-length instructions.
A64	The instruction set available when in AArch64 state.
AAPCS64	Procedure Call Standard for the ARM 64-bit Architecture (AArch64)
AArch32	The 32-bit general-purpose register width state of the ARMv8 architecture, broadly compatible with the ARMv7-A architecture.
AArch64	The 64-bit general-purpose register width state of the ARMv8 architecture.
ABI	Application Binary Interface: 1. The specifications to which an executable must conform in order to execute in a specific execution environment. For example, the *Linux ABI for the ARM Architecture*. 2. A particular aspect of the specifications to which independently produced relocatable files must conform in order to be statically linkable and executable. For example, the *C++ ABI for the ARM Architecture*, *ELF for the ARM Architecture*, …
ARM-based	… based on the ARM architecture …
Floating point	Depending on context *floating point* means or qualifies: (a) floating-point arithmetic conforming to IEEE 754 2008; (b) the ARMv8 floating point instruction set; (c) the register set shared by (b) and the ARMv8 SIMD instruction set.
Q-o-I	Quality of Implementation – a quality, behavior, functionality, or mechanism not required by this standard, but which might be provided by systems conforming to it. Q-o-I is often used to describe the tool-chain-specific means by which a standard requirement is met.
SIMD	Single Instruction Multiple Data – A term denoting or qualifying: (a) processing several data items in parallel under the control of one instruction; (b) the ARM v8 SIMD instruction set: (c) the register set shared by (b) and the ARMv8 floating point instruction set.
SIMD and floating point	The ARM architecture's SIMD and Floating Point architecture comprising the floating point instruction set, the SIMD instruction set and the register set shared by them.
SVE	Scalable Vector Extension
T32	The instruction set named *Thumb* in the ARMv7 architecture; T32 uses 16-bit and 32-bit instructions.

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ARM Contract reference LEC-ELA-00081 V2.0 AB/LS (9 March 2005)

2 OVERVIEW

The ABI for the ARM 64-bit architecture specifies the use of DWARF 3.0 format debugging data. For details of the base standard see [GDWARF].

The ABI for the ARM 64-bit architecture gives additional rules for how DWARF 3.0 should be used, and how it is extended in ways specific to the ARM 64-bit architecture. The following topics are covered in detail:

- The enumeration of DWARF register-numbers for use in .debug_frame and .debug_info sections (*§3.1*).
- The definition of *Canonical Frame Address* (CFA) used by this ABI (*§3.2*).

3 ARM-SPECIFIC DWARF DEFINITIONS

3.1 DWARF register names

[GDWARF] *§2.6.1, Register Name Operators*, suggests that the mapping from a DWARF register name to a target register number should be defined by the ABI for the target architecture. DWARF register names are encoded as unsigned LEB128 integers.

DWARF register name	AArch64 register name	Description	See note
0-30	X0-X30	64-bit general registers	1
31	SP	64-bit stack pointer	
32	*Reserved*		
33	ELR_mode	The current mode exception link register	
34-45	*Reserved*		
46	VG	64-bit SVE Vector granule pseudo register	2, 3
47	FFR	VG×8-bit SVE first fault register	4
48-63	P0-P15	VG×8-bit SVE predicate registers	4
64-95	V0-V31	128-bit FP/Advanced SIMD registers	5, 7
96-127	Z0-Z31	VG×64-bit SVE vector registers	6, 7

Notes:

1. The size of a general register is to be taken from context. For instance in a `.debug_info` section if the `DW_AT_location` attribute of a variable is `DW_OP_reg0` then the number of significant bits in the register is determined by the variable's `DW_AT_type` attribute. If no context is available (for example in `.debug_frame` or `.eh_frame` sections) then the register number refers to a 64-bit register.
2. The value of the SVE vector granule pseudo register is an even integer in the range 2 to 32. The value of the register is the available size in bits of the SVE vector registers in the current call frame divided by 64.
3. The SVE vector granule pseudo register enables the construction of DWARF expressions that require the use of the current vector length, such as the location of saved SVE predicate and vector registers on the stack using the DWARF stack frame operator `DW_CFA_expression`.

4. The available size of a SVE predicate register and the first fault register is VG×8-bits.
5. In a similar manner to the general register file the size of an FP/Advanced SIMD register is taken from some external context to the register number. If no context is available then the only the least significant 64 bits of the register are referenced. In particular this means that the most significant part of a SIMD register is unrecoverable by frame unwinding.
6. The available size of the SVE vector registers is VG×64-bits.
7. The architecture defines that the FP/Advanced SIMD registers (V registers) overlap with the SVE vector registers (Z registers). A given V register is mapped to the low 128-bits of the corresponding Z register.

   The DWARF call frame instructions do not explicitly specify the size of a register; this is implicit in the definition of the register. As a consequence the V registers and Z registers have been allocated separate DWARF register number ranges which have their own definition for the size of these registers.

   When searching the call frame information table for either a V register or a Z register a consumer must take into account the aliasing between the V and Z registers.

3.2 Canonical Frame Address

The term Canonical Frame Address (CFA) is defined in [GDWARF], §6.4*, Call Frame Information*.

This ABI adopts the typical definition of CFA given there.

- The CFA is the value of the stack pointer (sp) at the call site in the previous frame.

3.3 Common Information Entries

The DWARF virtual unwinding model is based, conceptually, on a tabular structure with one column for each target register ([GDWARF], *§6.4.1, Structure of Call Frame Information*). A `.debug_frame` Common Information Entry (CIE) specifies the initial values (on entry to an associated function) of each register.

The variability of execution environments conforming to the ARM architecture creates a problem for this model. A producer cannot reliably enumerate all the registers in the target. For example, an integer-only function might be included in one executable file for use in execution environments with floating-point and another for use in environments without. Therefore, it must be acceptable for a producer not to initialize, in a CIE, registers it does not know about. This generates an obligation on consuming debuggers to default missing initial values.

Note the following obligations on producers and consumers of CIEs:

1. Consumers must default the CIE initial value of any target register not mentioned explicitly in the CIE.
   - Callee-saved registers (and registers intentionally unused by the program, for example as a consequence of the procedure call standard) should be initialized as if by `DW_CFA_same_value`, other registers as if by `DW_CFA_undefined`.
     A debugger can use built-in knowledge of the procedure call standard or can deduce which registers are callee-saved by scanning all CIEs.
   - The VG pseudo register should be initialized as if by `DW_CFA_same_value`.
2. To allow consumers to reliably default the initial values of missing entries by scanning a program's CIEs, without recourse to built-in knowledge, producers must identify registers not preserved by callees, as follows.
   - If a function uses any register from a particular hardware register class (e.g. ARM core registers), its associated CIE must initialize all the registers of that class that are not callee-saved to `DW_CFA_undefined`.

(As an optimization, a producer need not initialize registers it can prove cannot be used by any associated functions and their descendants. Although these are not callee-saved, they are not callee-used either).

- If a function uses a callee-saved register R, its associated CIE must initialize R using one of the defined value methods (not `DW_CFA_undefined`).